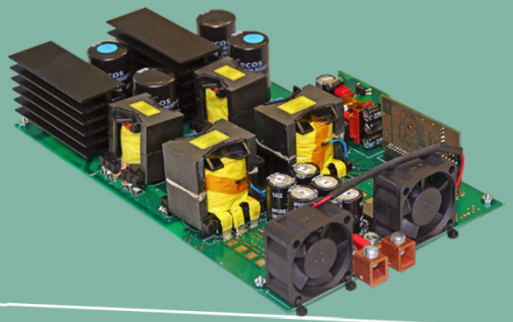
3kW Dual Phase LLC converter with full digital control



Francesco Di Domenico
IFAT PMM ACDC AE
HV DC/DC Converters Applications

April 2016

Contents

1 System Background and Most Relevant Spec Requirements

2 Design Concept

3 Advanced Features

4 Efficiency Results

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Target Application: Telecom HP SMPS





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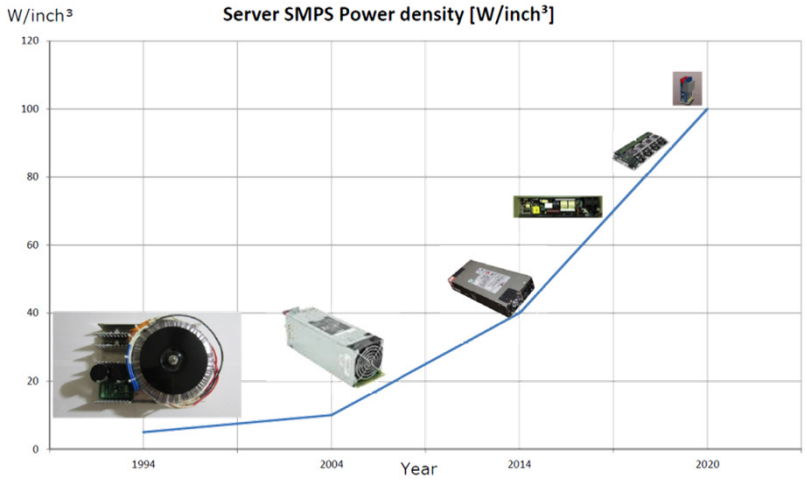
Major Trends in HP SMPS applications

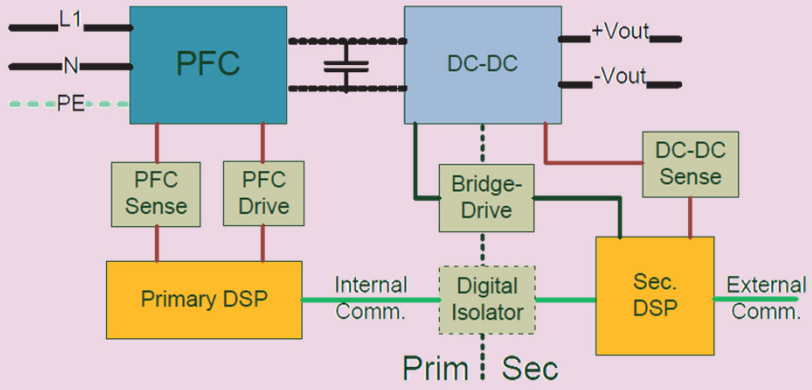
Power Density



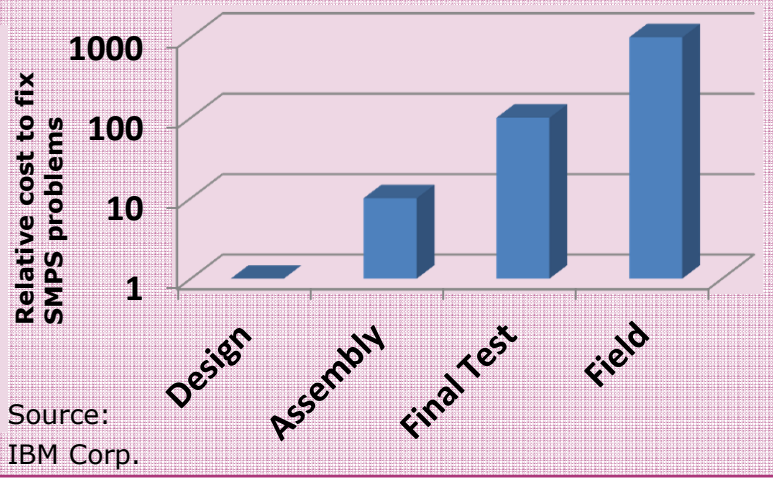
Economies of scale



Digital Control



Reliability



Source:
IBM Corp.

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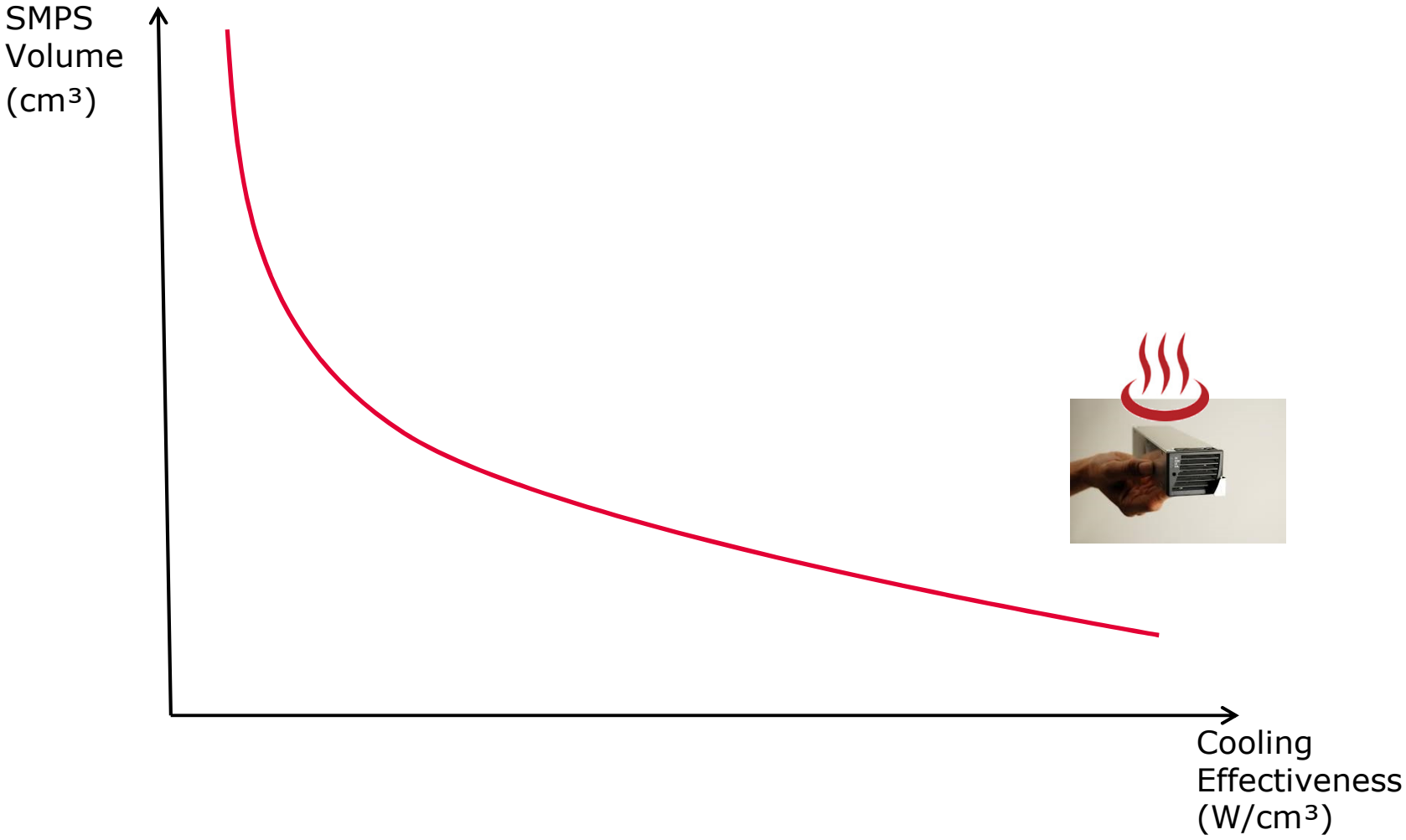
Trend: Power Density
Cooling Volume vs. Cooling Effectiveness



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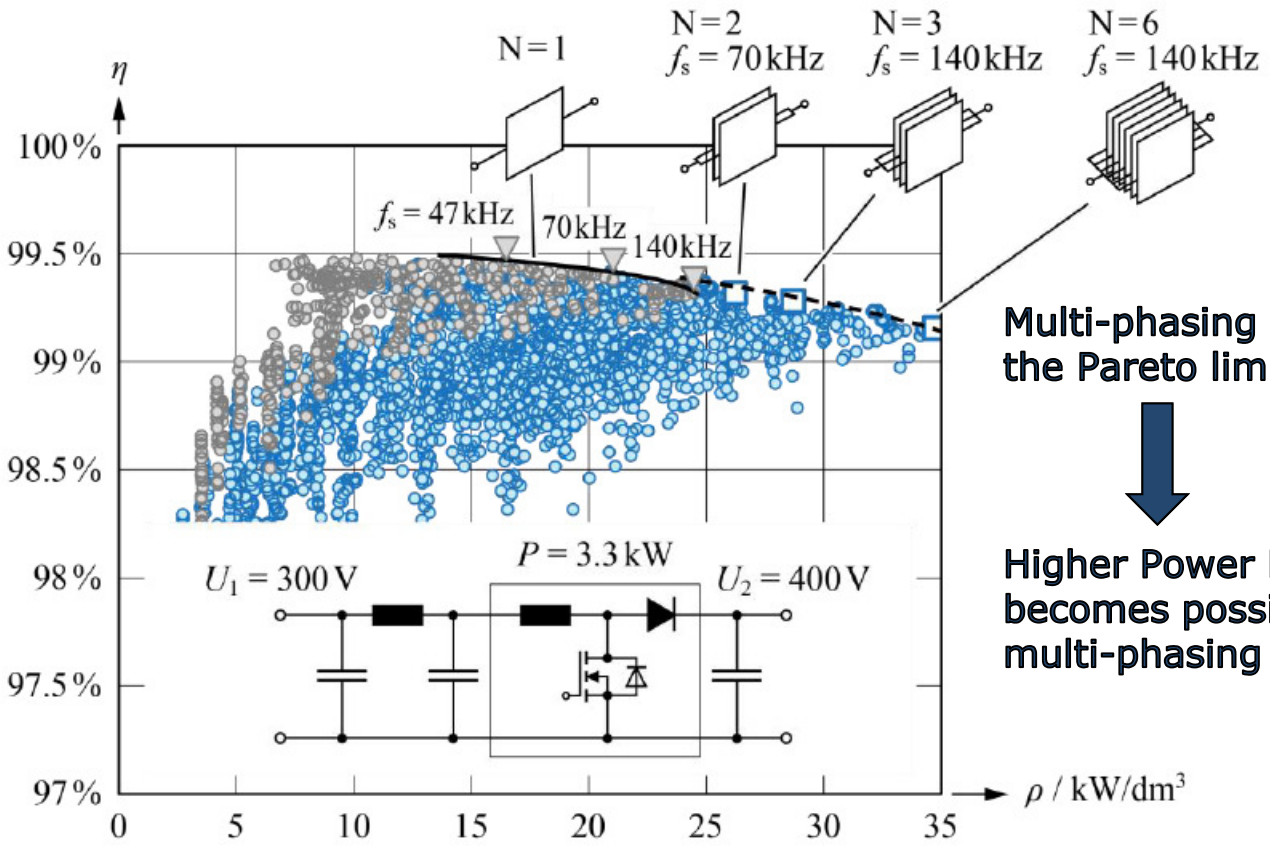
Efficiency/Power density Pareto limit



Multi-phasing shifts the Pareto limit!

Higher Power Density becomes possible with multi-phasing approach!

[1kW/dm³=16.38W/inch³]

Source: Prof. Kolar – ETH Zurich

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Telecom SMPS Key Features: Flat Efficiency Plot



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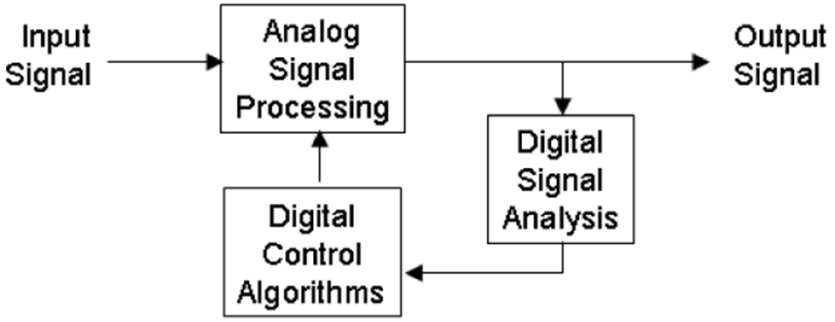
Telecom SMPS Key Features

- Highest efficiency in minimum space



- Digital Control & Communication



CAN PMBus

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Telecom SMPS Key Features

- Modular approach (power shelf)



- High MTBF requirements: >300.000hours at Tamb=25°C (according to SR-332 calculation methodology)

Telcordia®

ETSI

World Class Standards

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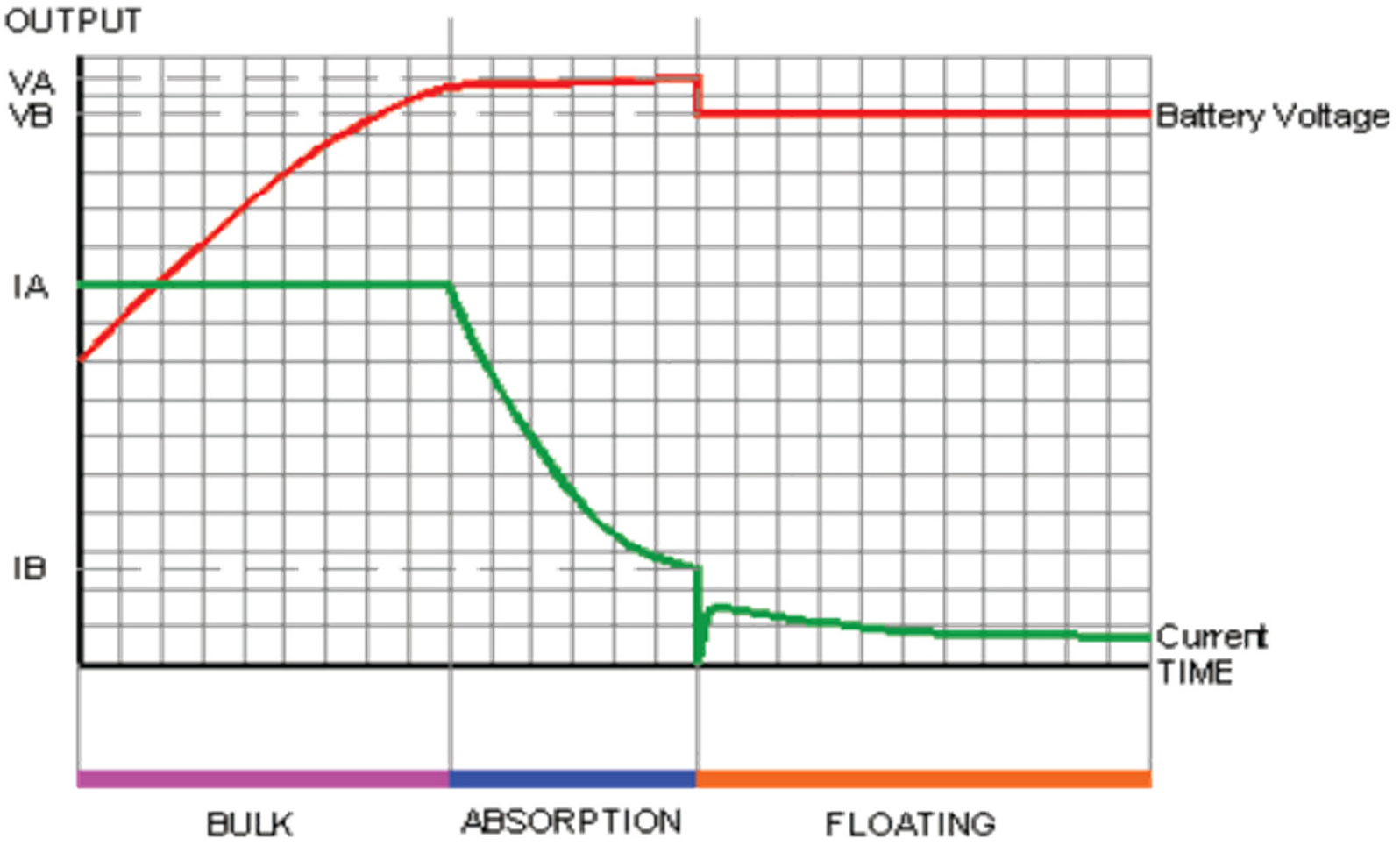
Telecom SMPS Key features

- Accurate control of the charge curve



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Technical Specifications

Technical Specification

44-58V/55A Isolated Dual Phase Half Bridge LLC Converter

Prepared by: Francesco Di Domenico
IFAT PMM APS SE AC – HV DC/DC Converters Applications

Revision History:

Revision	Date	Originator	Comments
Draft	24.01.2014	*Francesco Di Domenico*	**Initial Draft**
Rev. 1.0	27.02.2014	*Francesco Di Domenico*	**Definition of scope, In/Out regulation requirements, transient response, SR configuration, cooling and other minor changes/corrections**
Rev. 1.1	17.07.2014	*Francesco Di Domenico*	As per discussion in 17.07.2014 meeting
Rev. 1.2	06.08.2014	*Matthias Tauer / FP*	As per discussion in 06.08.2014 telcon

Software Specification

44-58V/55A Isolated Dual Phase Half Bridge LLC Converter

Prepared by : Francesco Di Domenico — IFAT PMM ACDC AE
Sam Abdel-Rahman — IFNA PMM SMD AMR PMD Z

Revision History:

Revision	Date	Originator	Comments
Draft	03.02.2014	*Francesco Di Domenico*	**Initial Draft**
Rev 1.1	27.02.2014	*Sam Abdel-Rahman & Francesco Di Domenico*	**Software features/requirements concept**
Rev 1.2	22.07.2014	*Matthias Tauer / Finepower*	**Descriptions / implementations added**
Rev 1.3	18.06.2015	Matthias Tauer / Finepower	**Final implementation and explanations for algorithms added**

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Target of the 3kW Dual Phase LLC Design

Performance

Modularity



Flat Efficiency

Reliability

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Relevant items in the technical spec

- Overview of technical specification:
  - Input voltage: $380V_{DC_nom}$ ($350\text{-}410V_{DC}$)
  - Output voltage: $54.3V_{DC_nom}$ ($44\text{-}58V_{DC}$)
  - Output current: 0A-55A
  - Topology:
    - Two phases 1500W HB LLC
    - Transformer in center tap configuration on secondary side

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Efficiency target

Pout	Minimum Required
10%Pmax=300W	95%
50%Pmax=1500W	98%
100%Pmax=3000W	97.5%

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Relevant items in the technical specs

- Full digital control (one microcontroller for both converter), microcontroller located on secondary side
- Prevention of hard commutation at following conditions:
  - Start-up (no-load, overload/short circuit)
  - Burst Mode
  - Output overload/short circuit
  - Dynamic load 0-100%
- Prevention of LLC capacitive load mode operation
- GUI
  - Visualization of relevant info about the converter's operation, including parameters measurements and fault flags
  - Allowing easy access to parameter changes
  - Remote Enable/Disable functions

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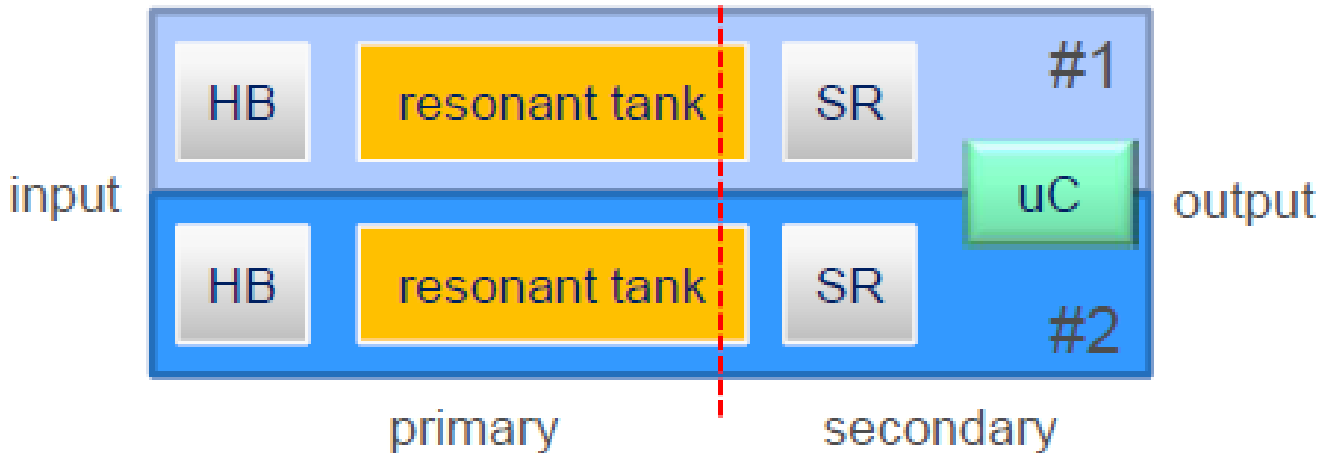
Design Concept



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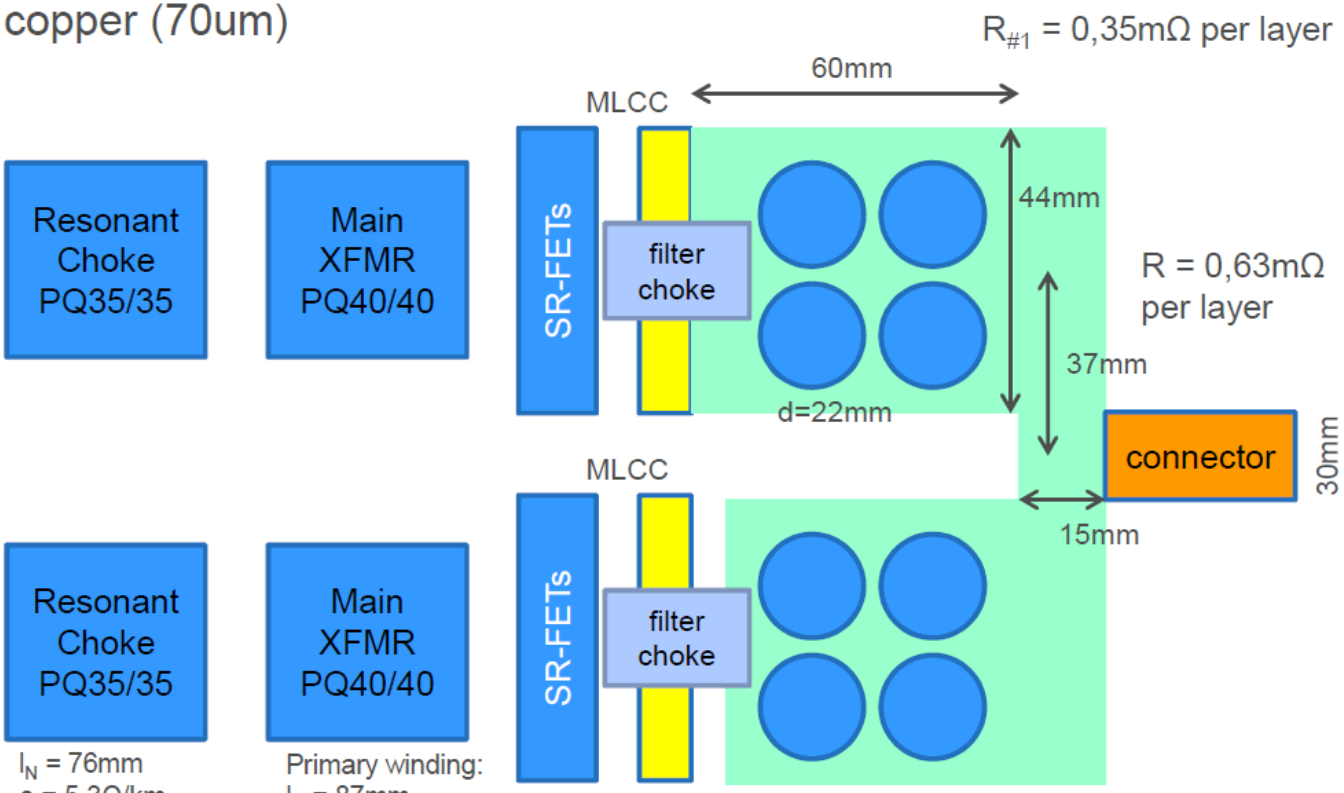
Basic components positioning in the PCB

4 layer PCB, 2oz copper (70um)



l_N = 76mm
ρ = 5,3Ω/km
Rcu = 4,03mΩ

Primary winding:
l_N = 87mm
ρ = 5,3Ω/km
Rcu = 6,5mΩ

Secondary winding:
l_N = 87mm
Acu = 22 x 0,25mm² = 5,5mm²
Rcu = 1,11mΩ

fine power®

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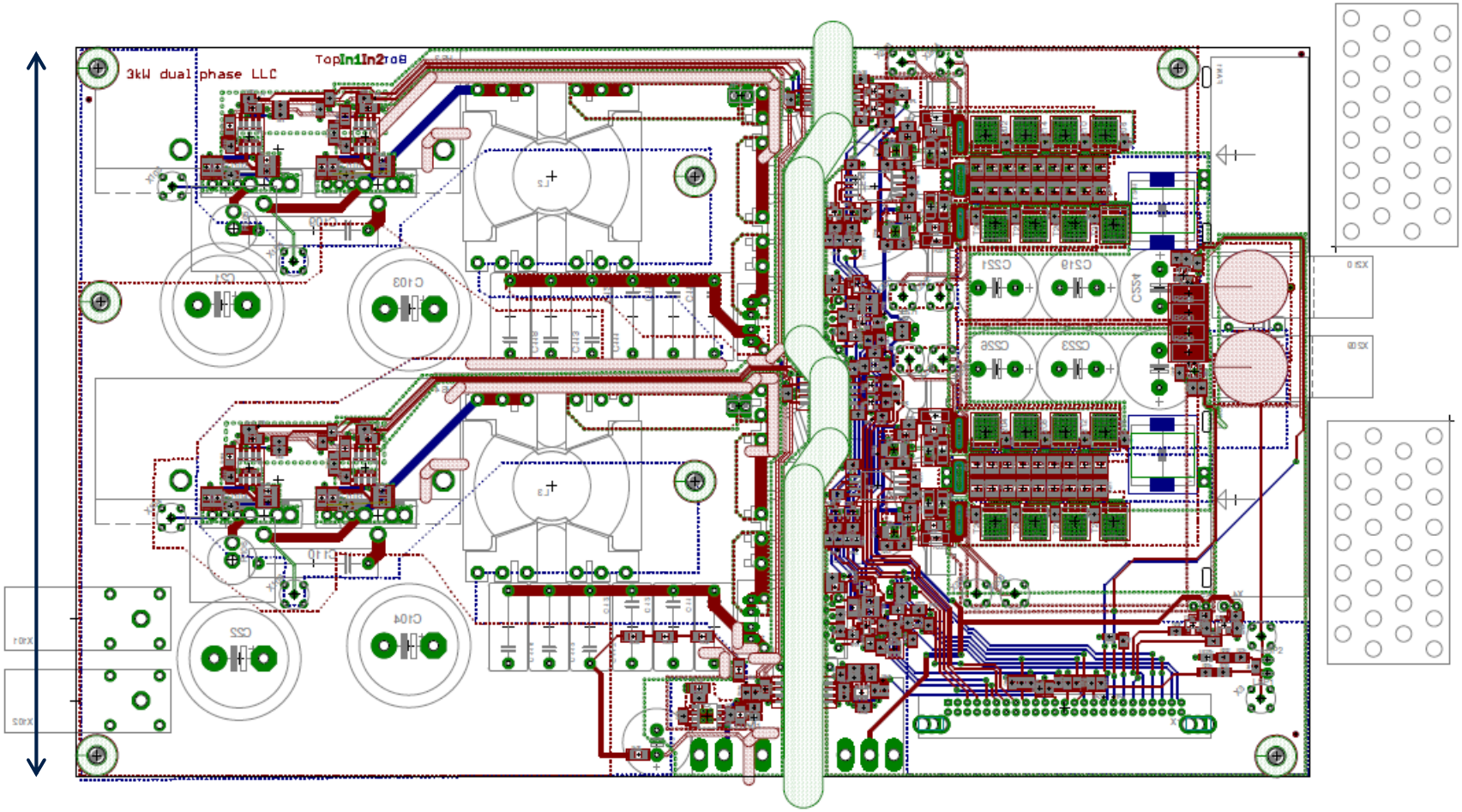
Main Power Board Layout



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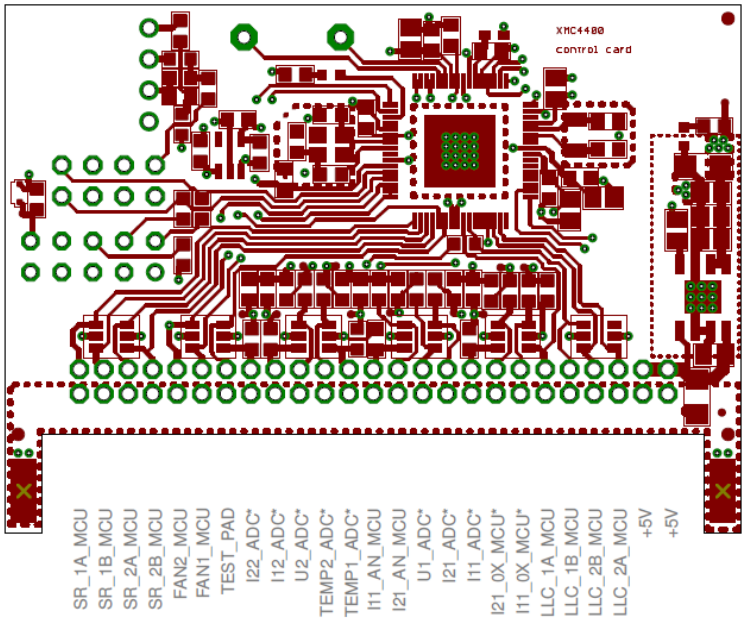
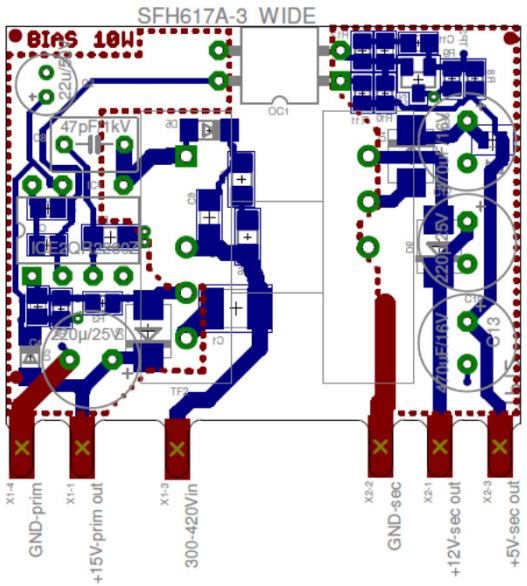
Two Daughter Boards



Microcontroller Board



Auxiliary Converter Board

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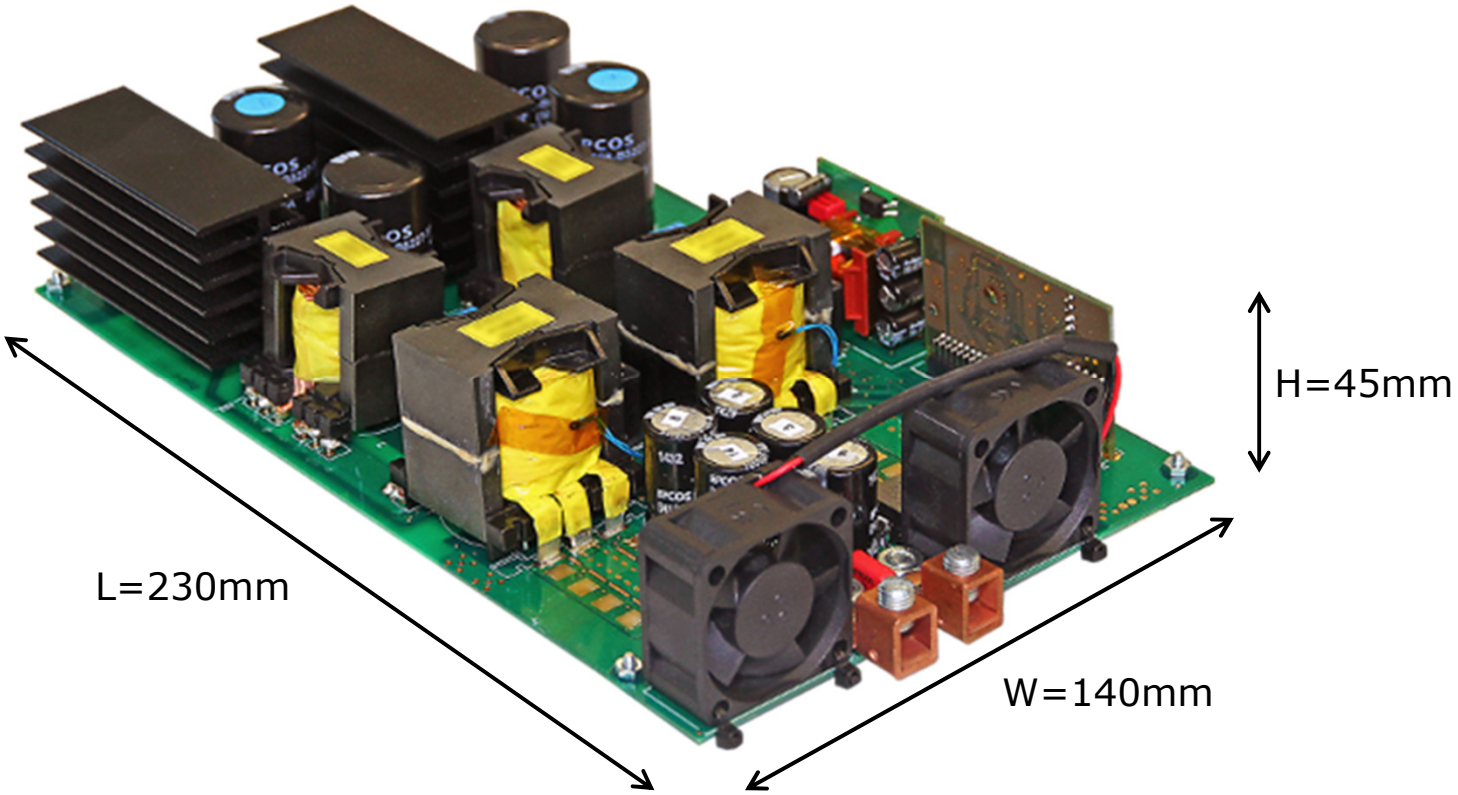
Final shape and overall dimensions



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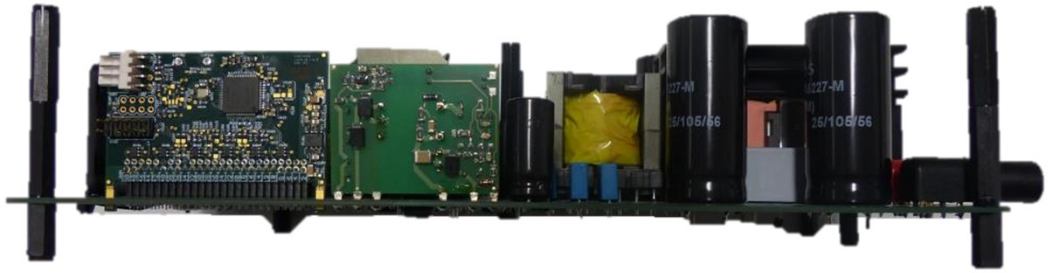
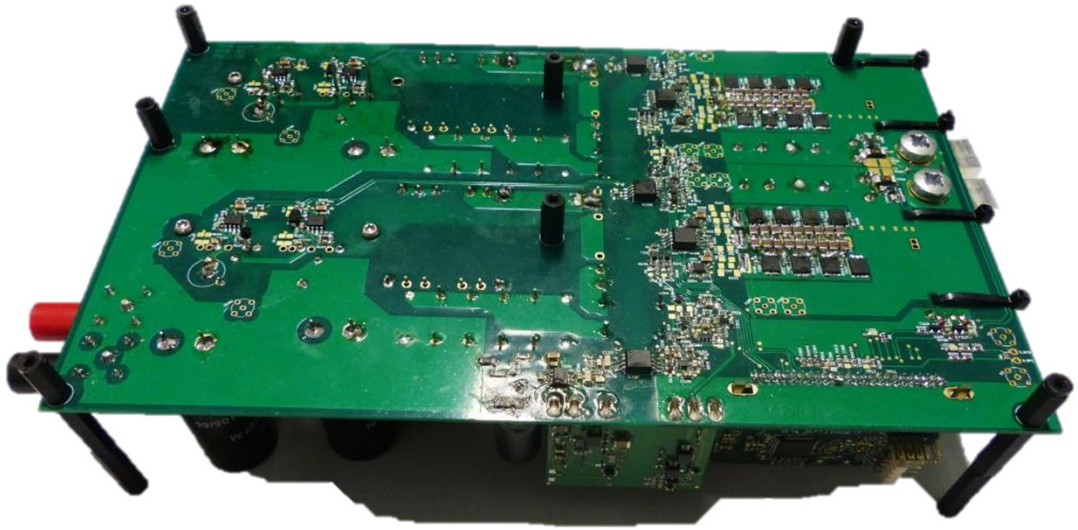
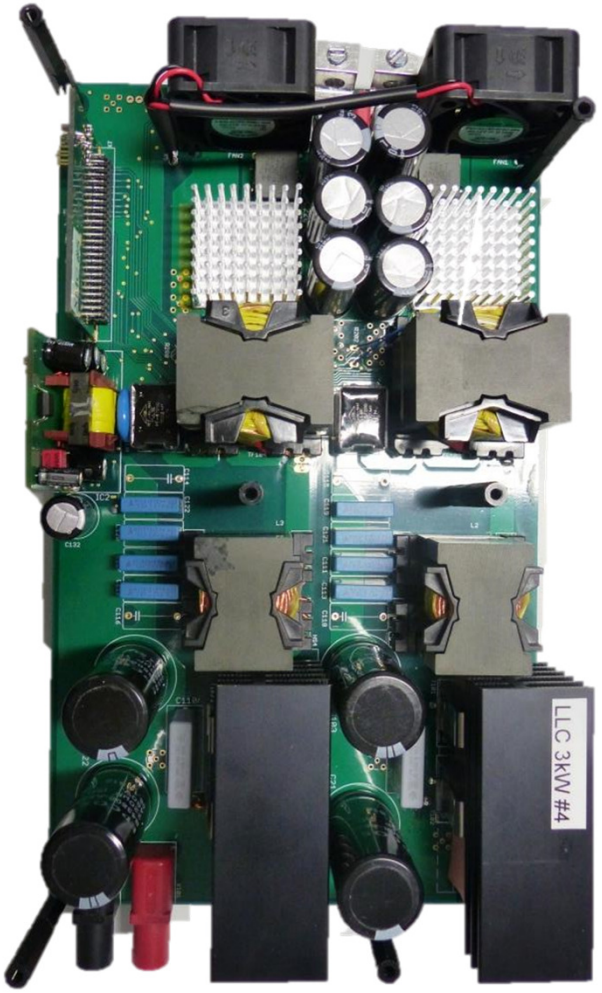
Board pictures







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Boards overview

Main features of each of the two phases	
V_{in}	380 V_{DC}
V_{out}	44 - 58 V_{DC}
I_{out_max}	28A
P_o	1.5 kW
$f_{res}=f_0$	125KHz
f_{min}	90Khz
f_{max}	200KHz
C_r	2x 66 nF
L_r	12 uH
L_m	62 uH

Primary HV MOSFETs
- **CoolMOS™ IPP60R040C7**

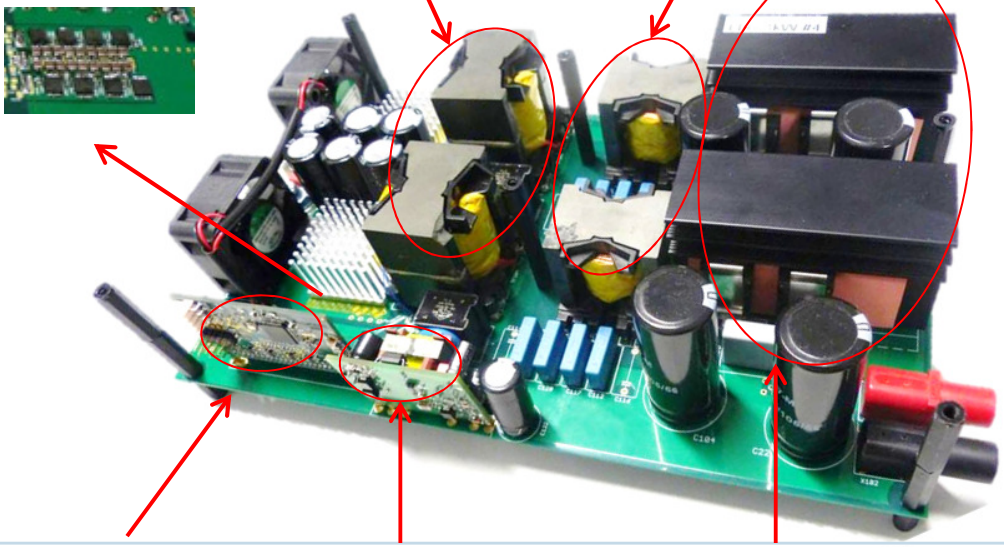
Reduced Gate Charge (Q_g)
- Reduced E_{off}
- High body diode ruggedness

SR MOSFETs
- **OptiMOS™ BSC093N15NS5**
- New generation
- Best FOM $R_{DS(on)}$ x Q_g
- Best FOM $R_{DS(on)}$ x Q_{oss}

Transformer
SP-PQ 40/40 core

Resonant inductor
SP-PQ 35/35 core

LV MOSFETs
BSC093N15NS5



LLC controller
Digital XMC4400

Bias QR Flyback controller
ICE2QR2280Z

HV MOSFETs
IPP60R040C7 TO-220
IPW60R040C7 TO-247

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Full Infineon Solution

- Primary HV MOSFETs:
  - **40mΩ 600V CoolMOS C7, triple pin-out (T0220, TO247, TO247-4)**
- Secondary SR LV MOSFETs
  - **150V, 9.3mΩ OptiMOS5 BSC093N15NS5**
- Primary MOSFETs driver:
  - **1EDI60N12AF**
- Secondary MOSFETs driver:
  - **2EDN7524R**
- Microcontroller (on a dedicated daughter card):
  - **XMC4400**
- Auxiliary Converter Controller/MOSFET (on a dedicated daughter card):
  - **ICE2QR2280Z**

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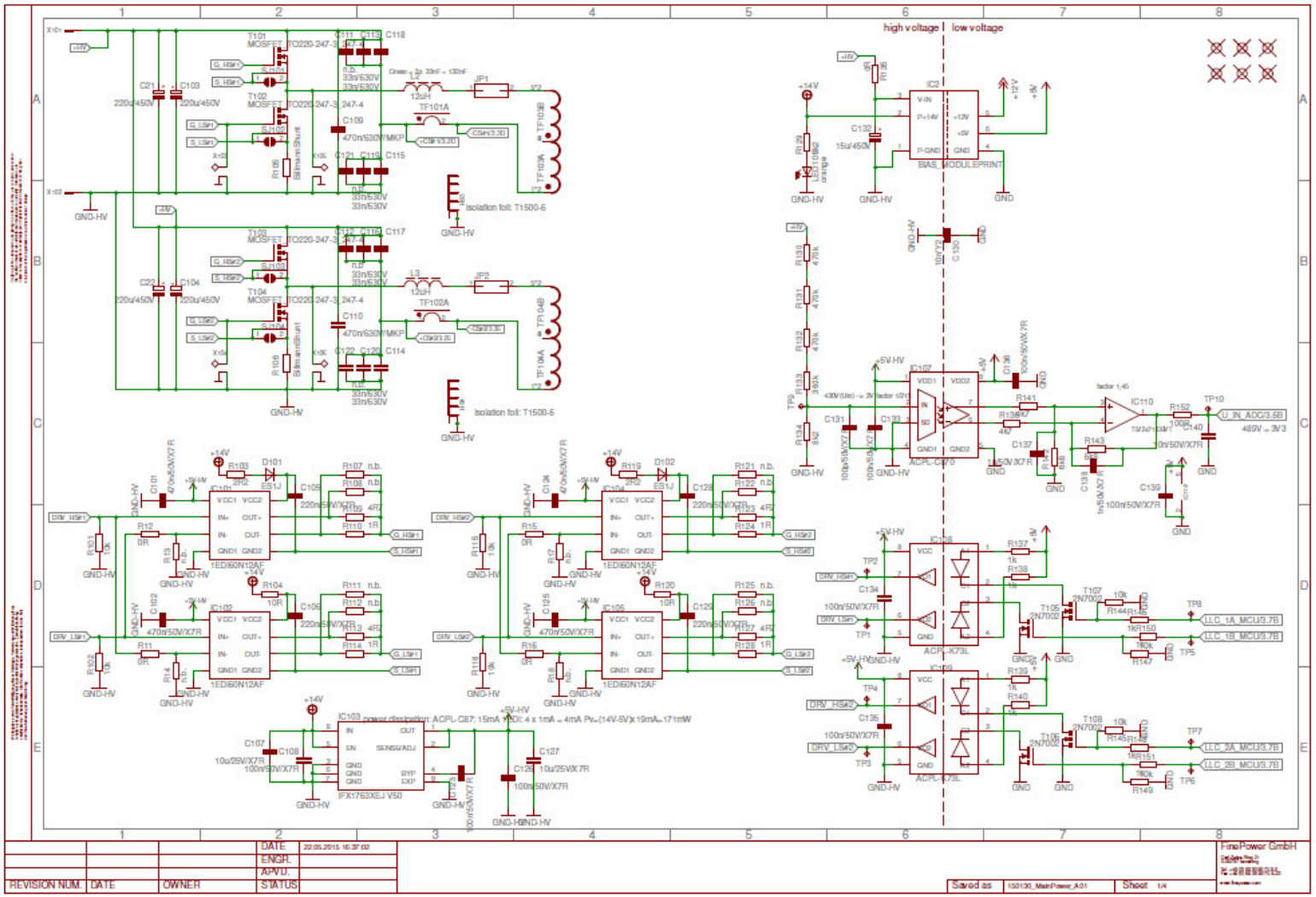
Main Board_1



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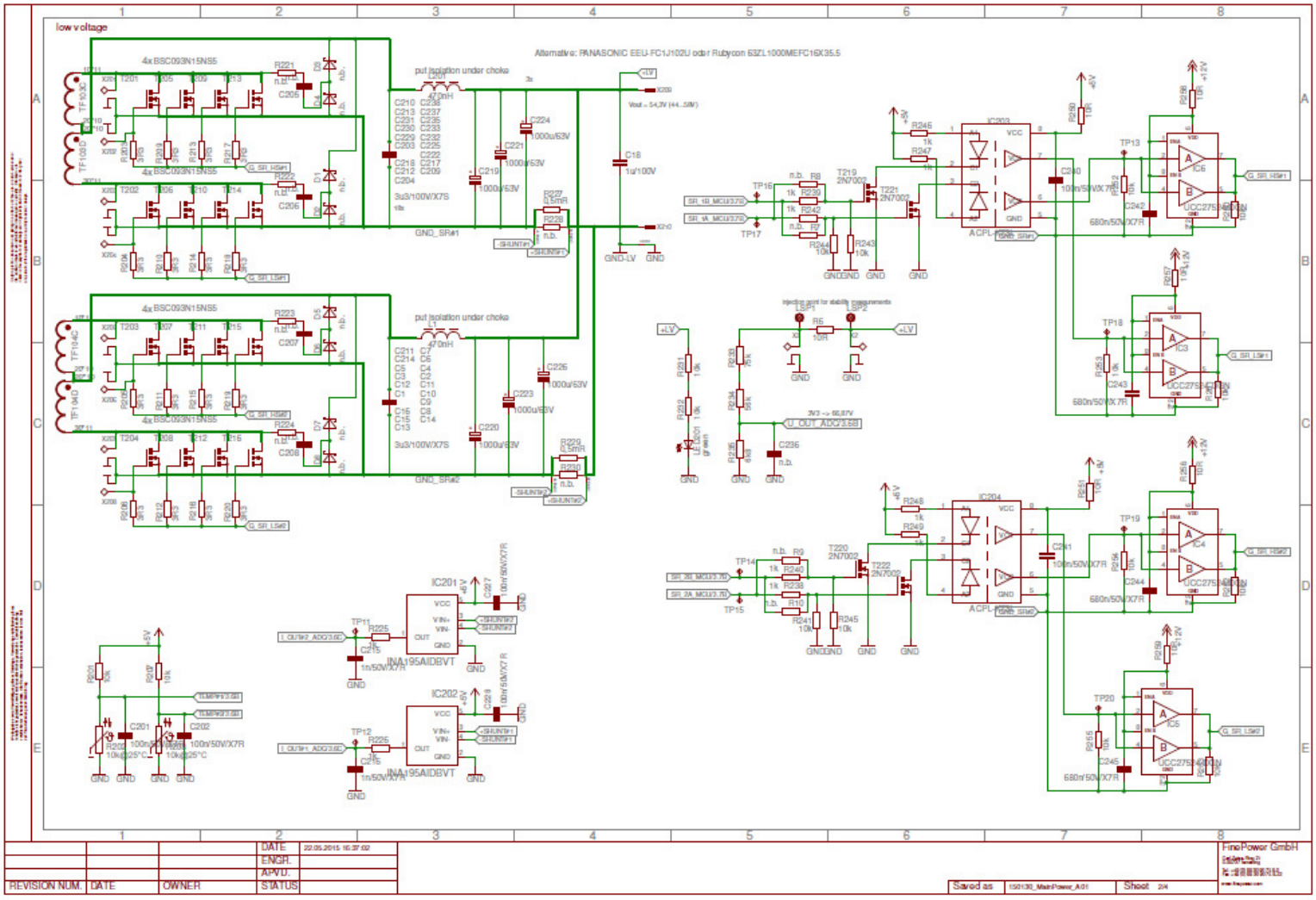
Main Board_2



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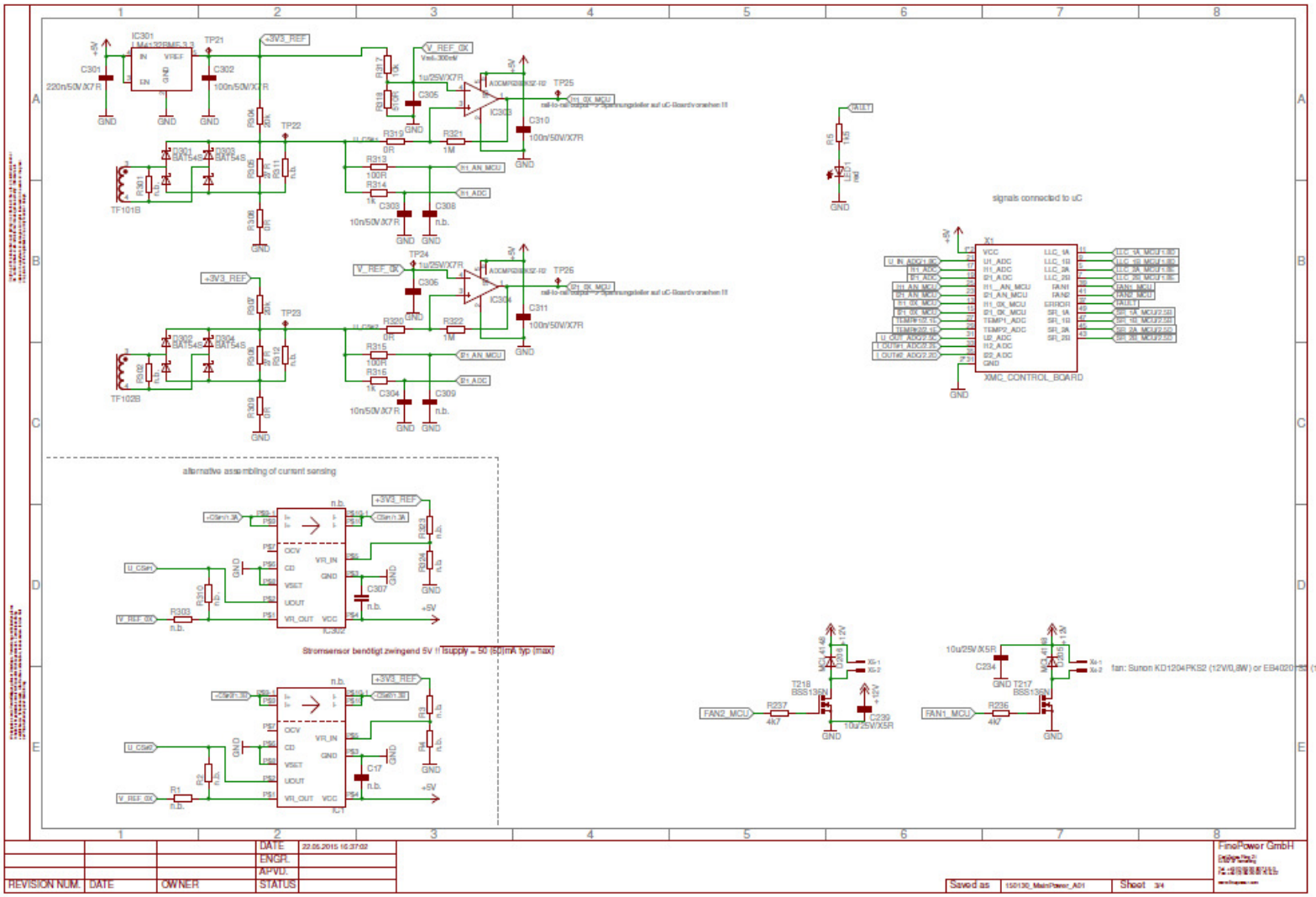
Main Board_3



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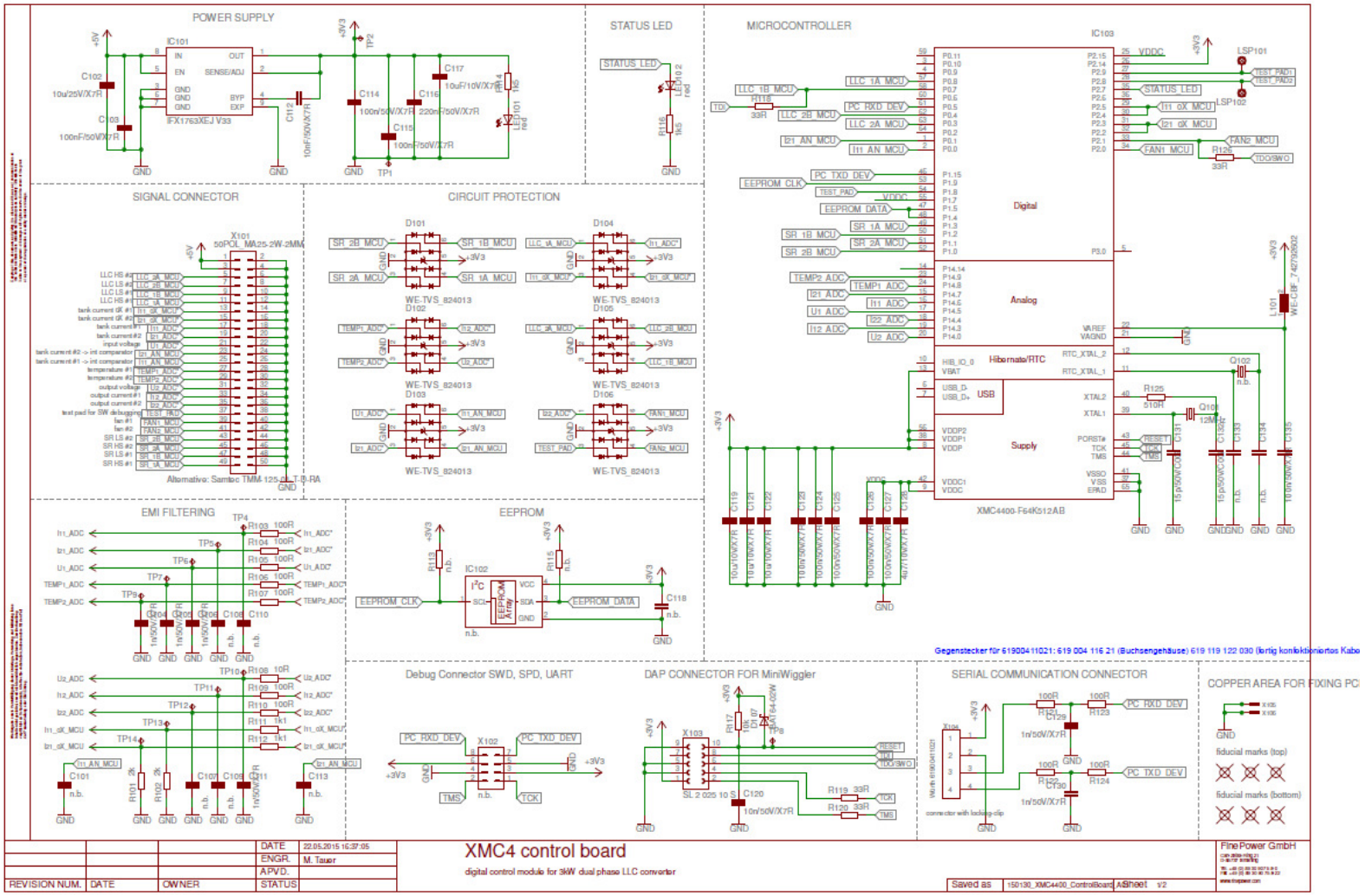
Control Board



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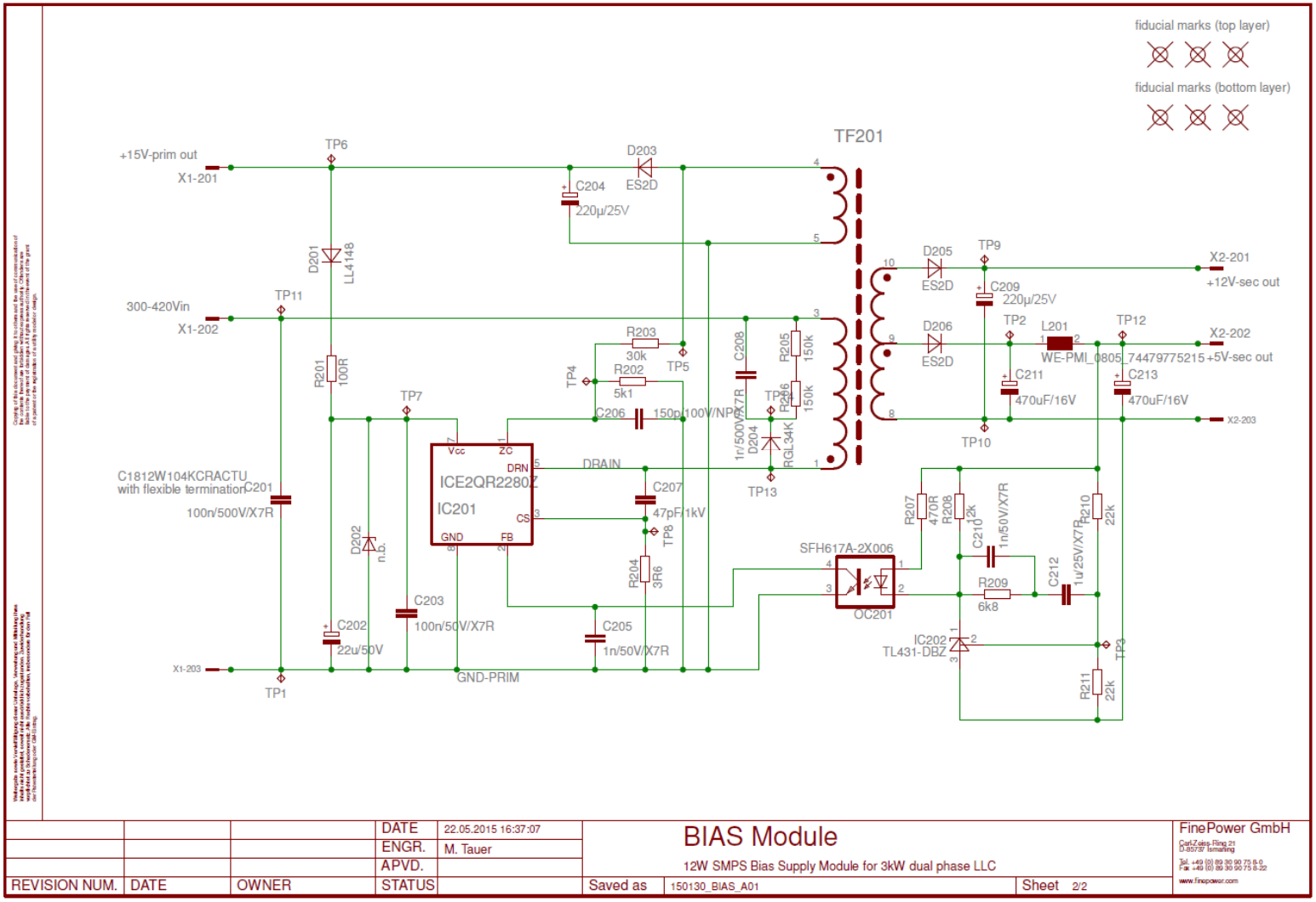
Bias Board



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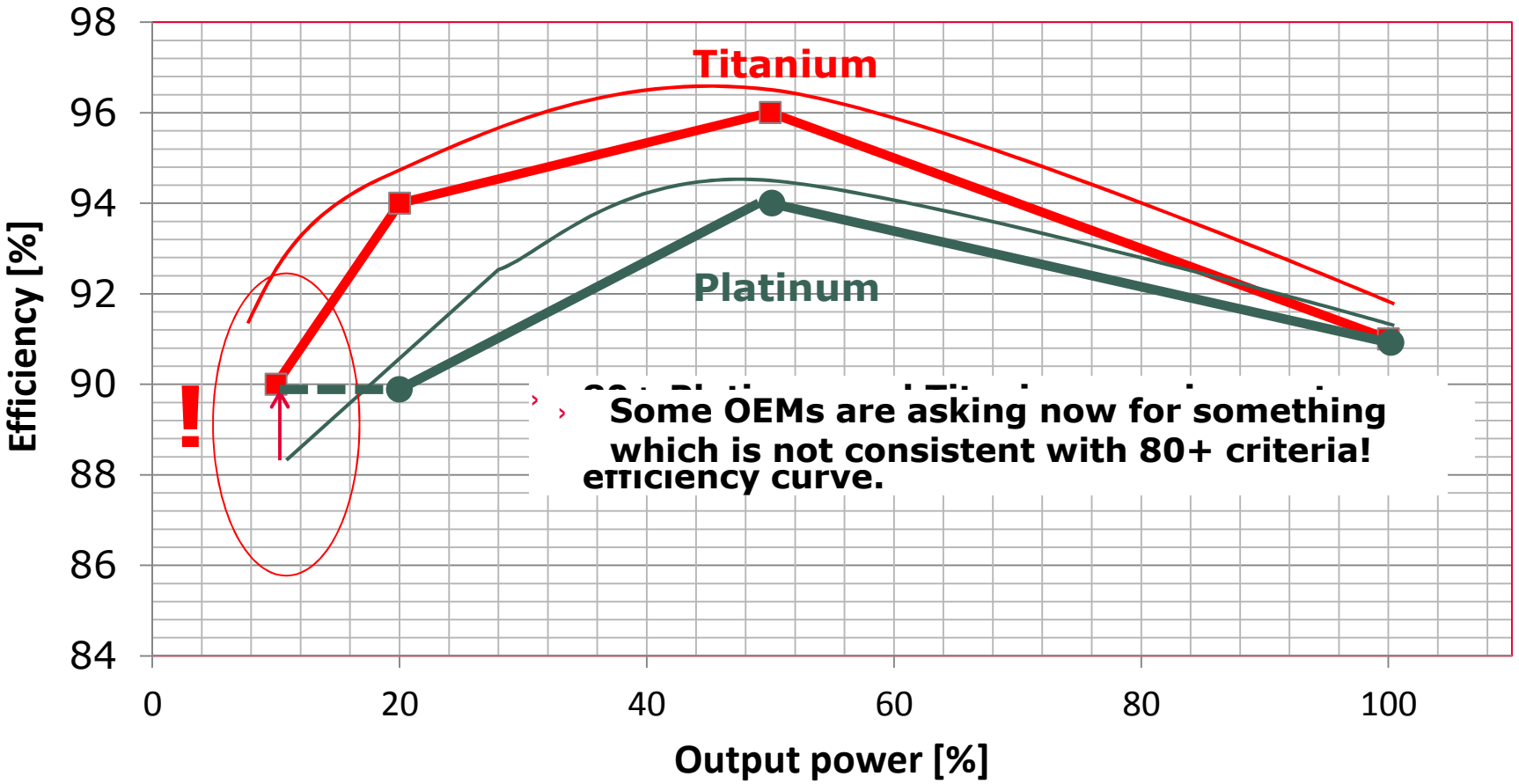
Trend: Load condition



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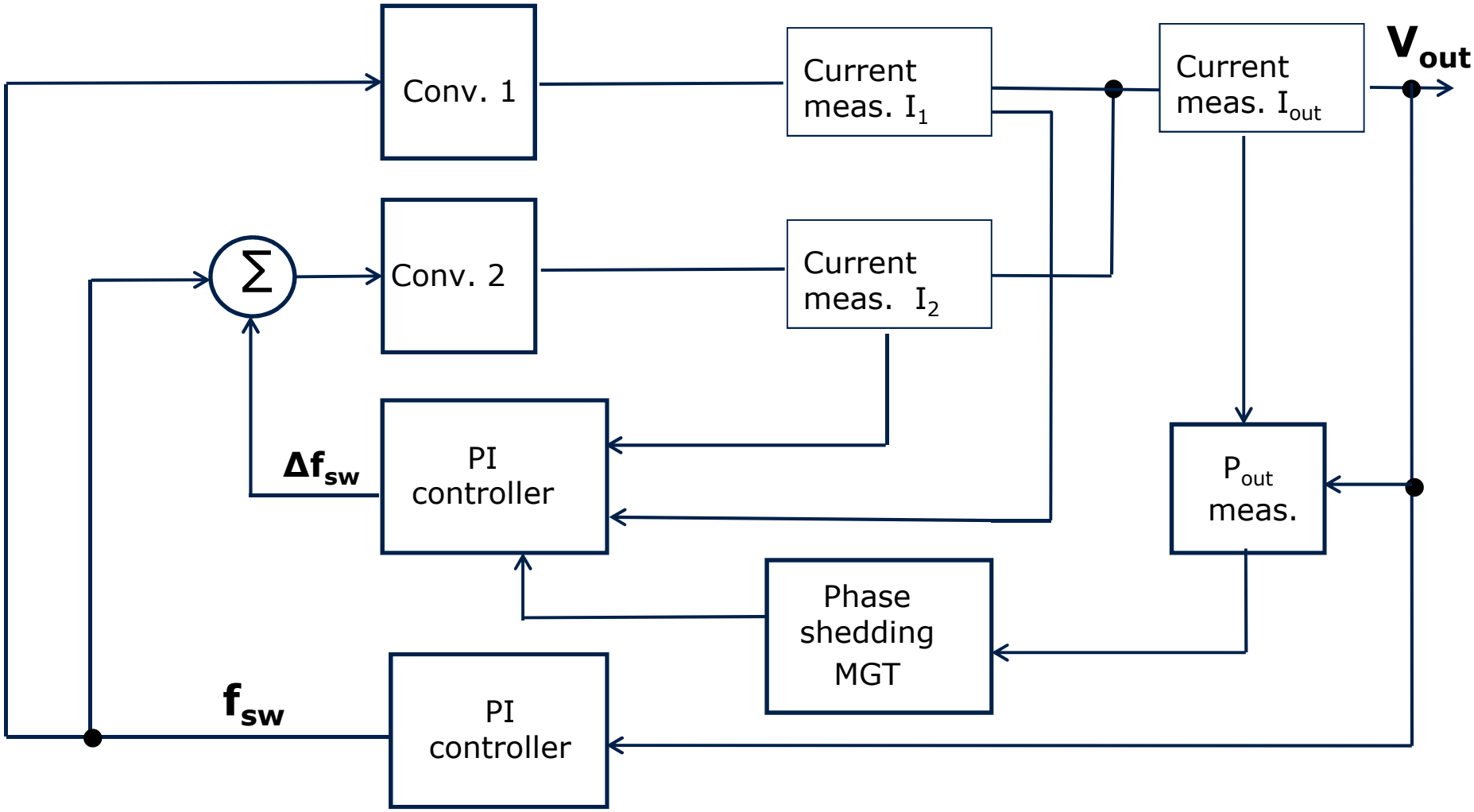
The digital current sharing and phase shedding



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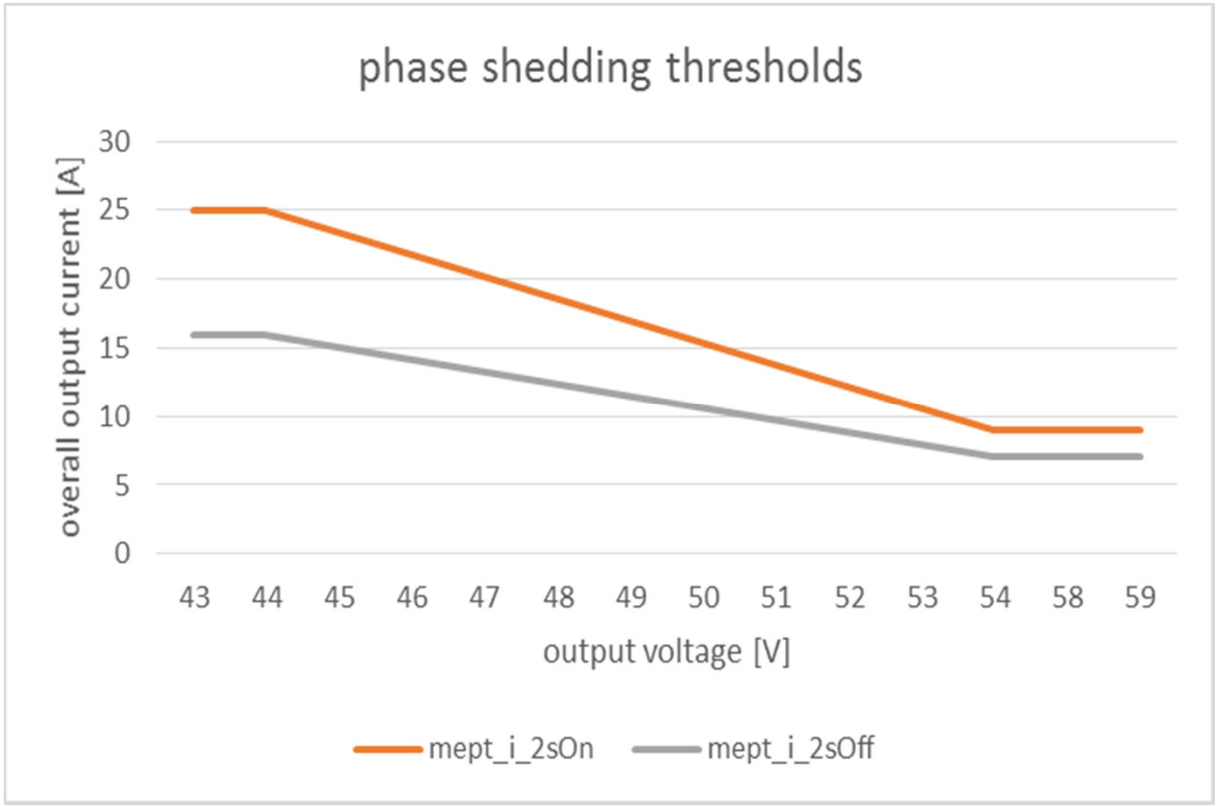
Phase shedding



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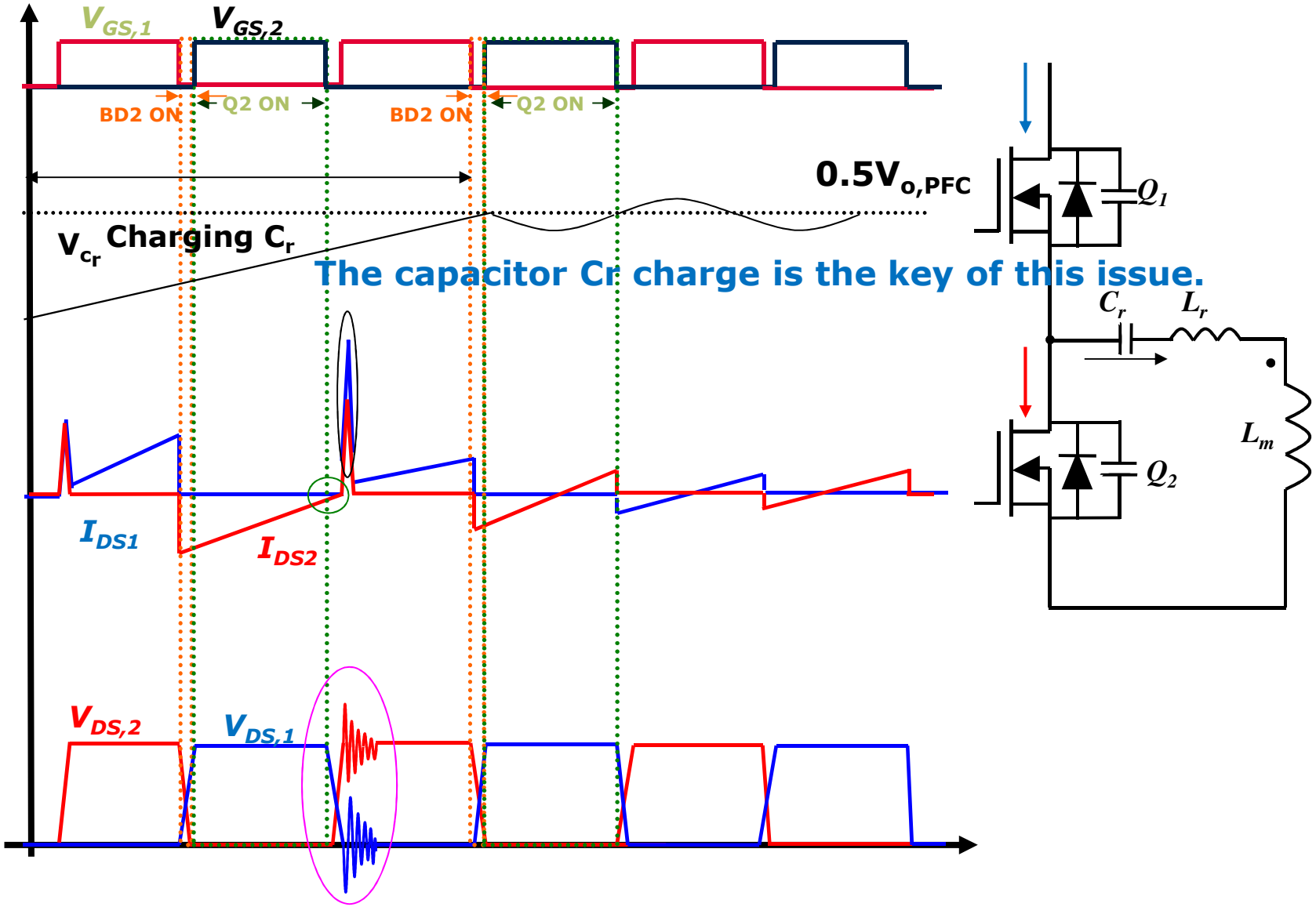
Typical Startup Hard Commutation Waveforms in HB resonant topology



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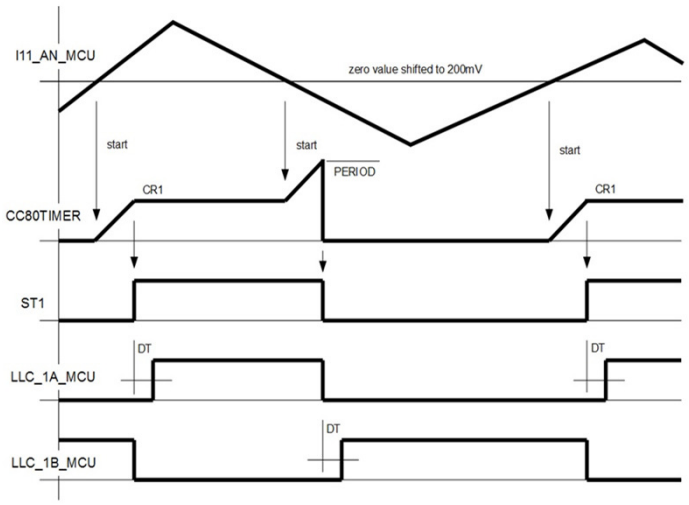
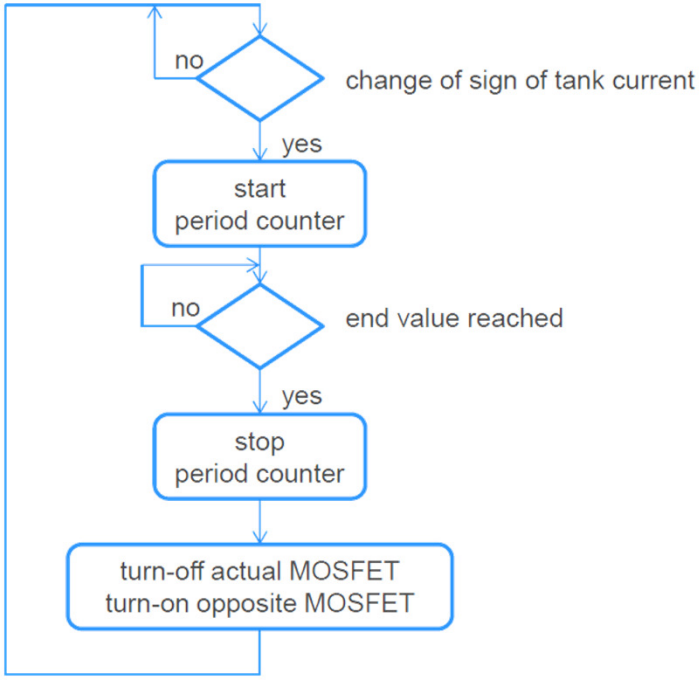
Hard Commutation prevention at Start-up

- Start-up time diagram
  - LLC HB PWM driven by zero current comparison
  - Current zero crossing „time“ is measured to ensure soft-transition to normal operation





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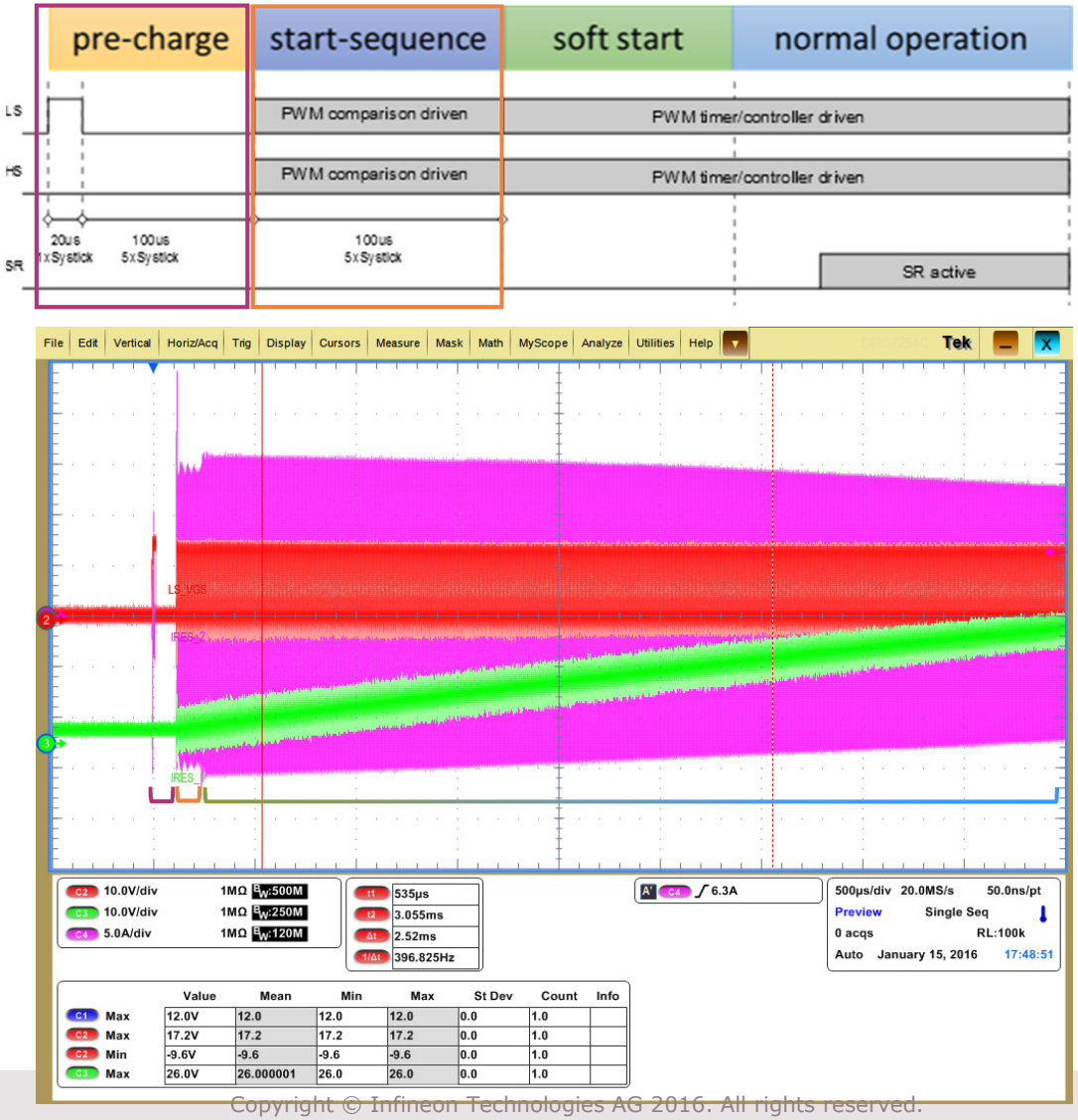
Complete Start-up sequence in 3kW Dual Phase LLC

- Operation of both stages is divided in 4 time slots



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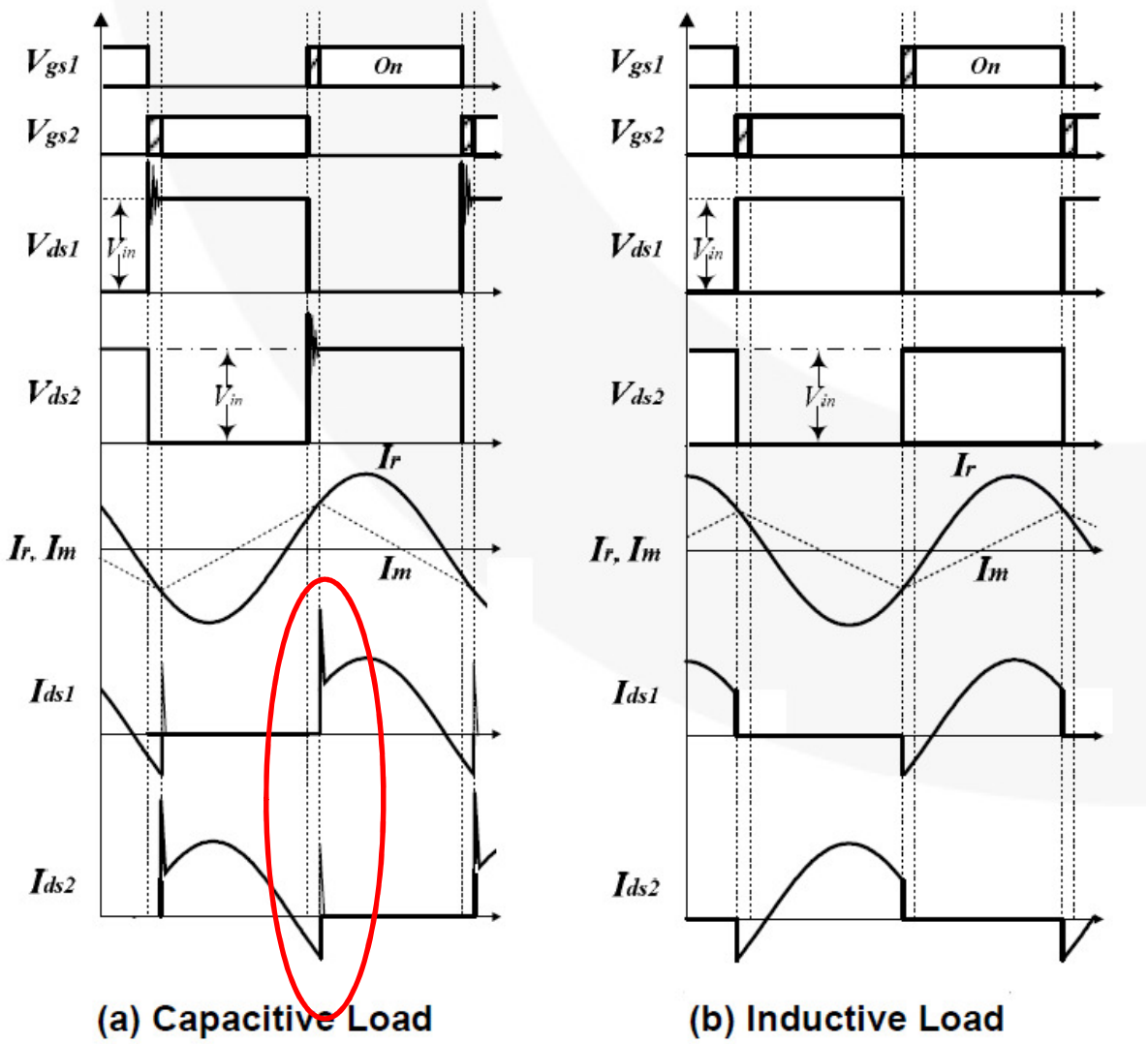
LLC Capacitive vs. Inductive Load operation



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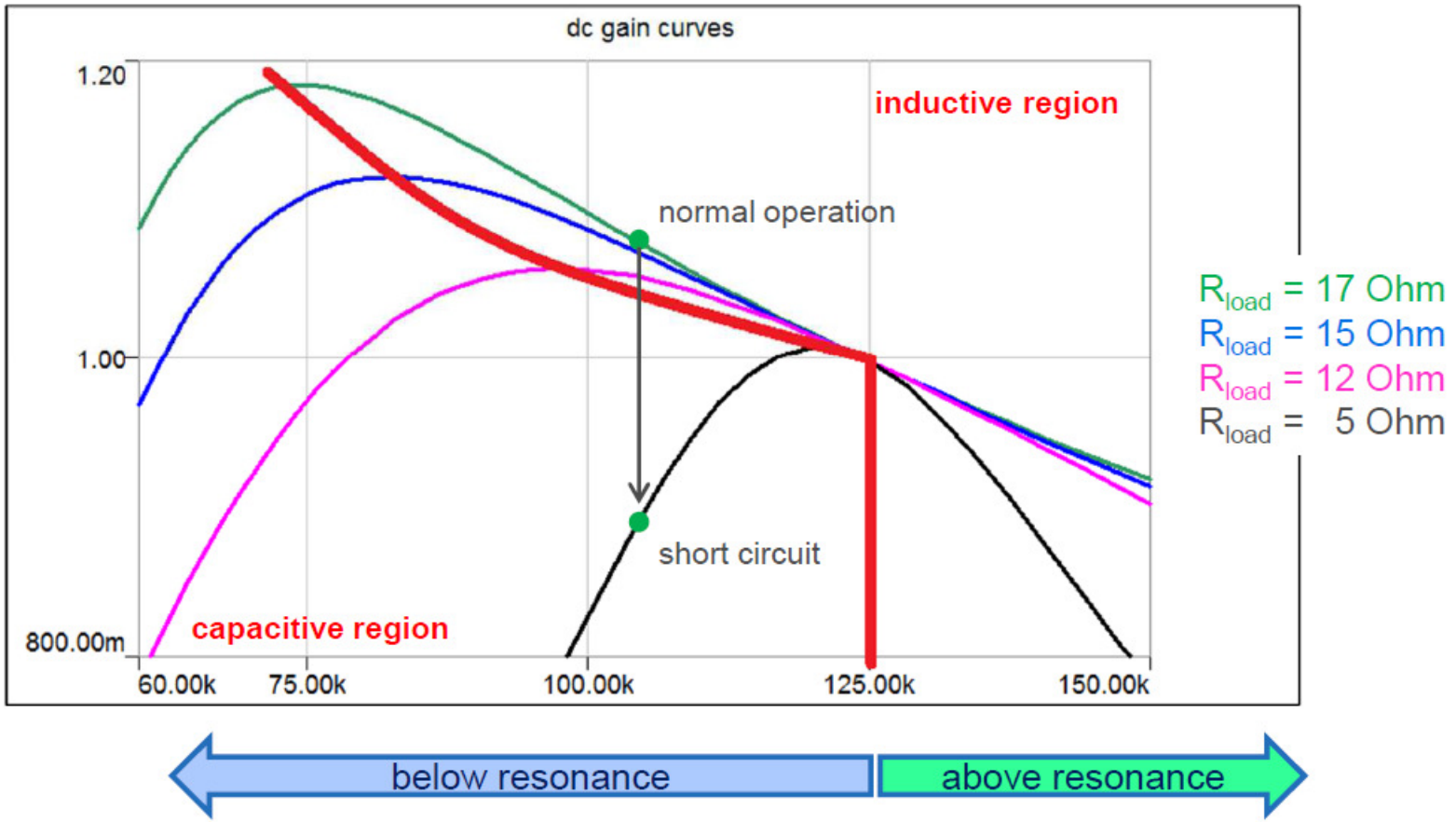
Output Short Circuit starting from operation below resonance



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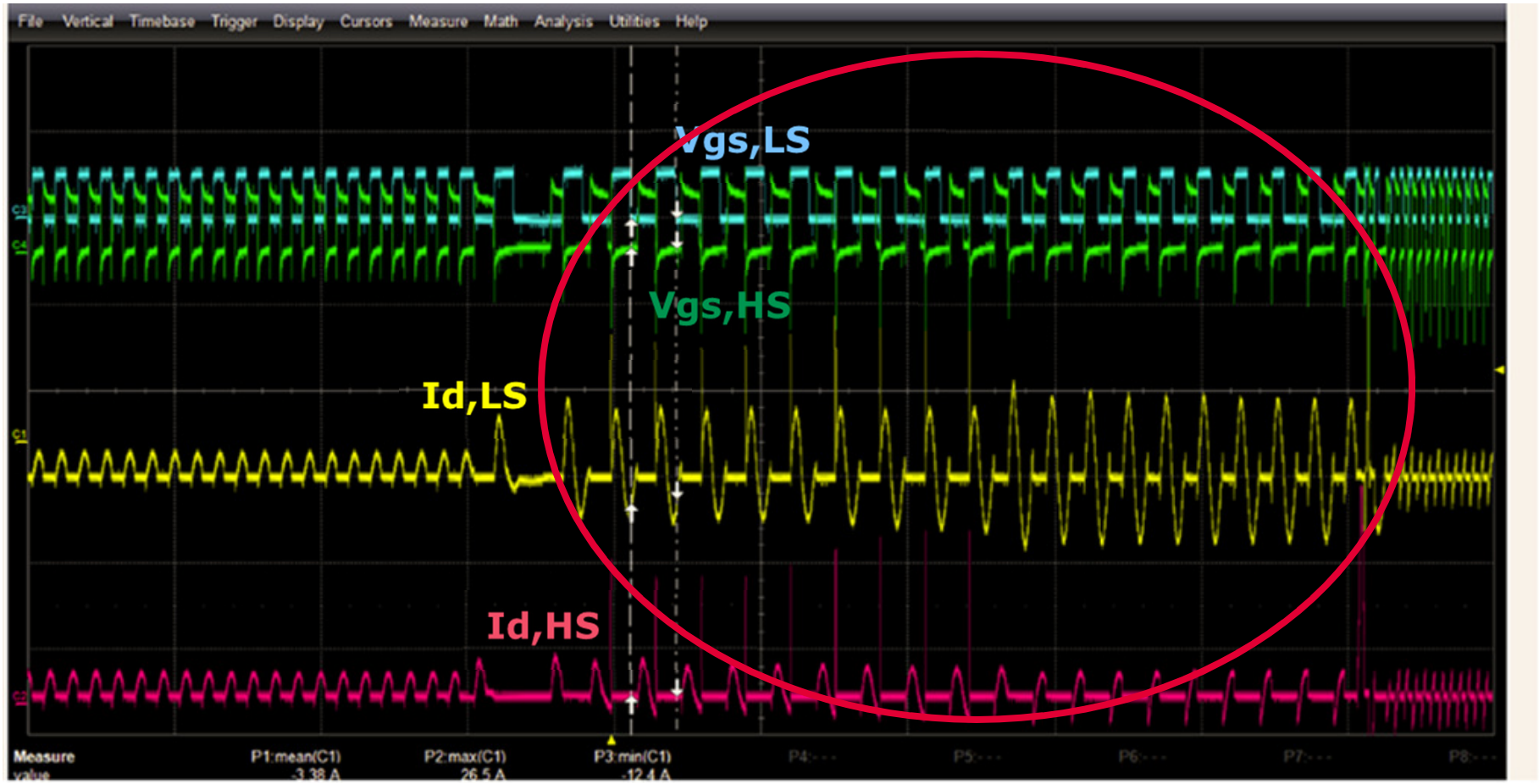
Typical Capacitive Load Mode at output short circuit test in SMPS without prevention



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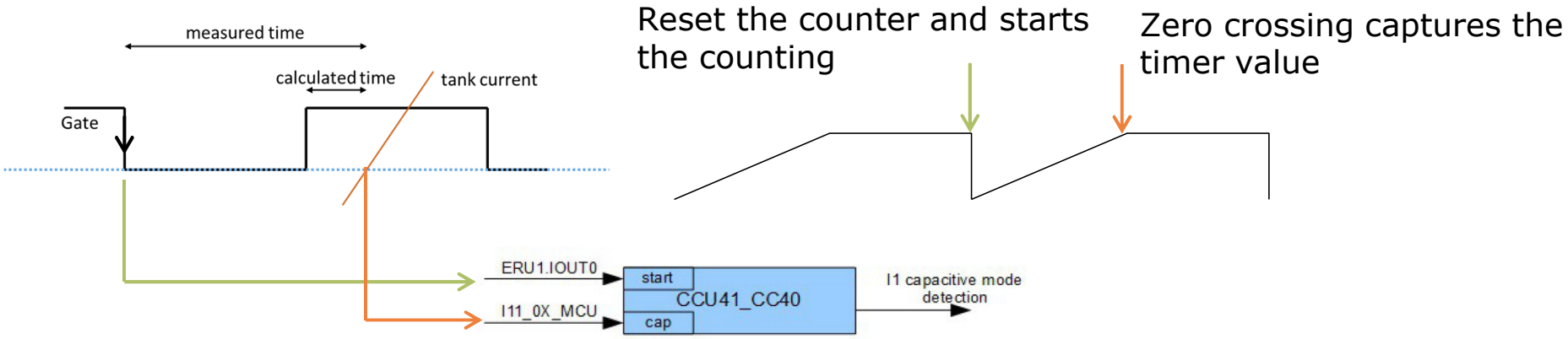
Capacitive mode detection/prevention

- Anti-capacitive mode procedure shows two protection levels
  - (1) Prediction: if phase shift between voltage and current gets closer to zero → increase switching frequency by decreasing output voltage target (ISR + main)
  - (2) Protection: if calculated time is zero or negative → shutdown the converter (ISR)
  - Prediction (1) can shutdown the converter if there are many successive tries of increasing the frequency (slow motion protection)



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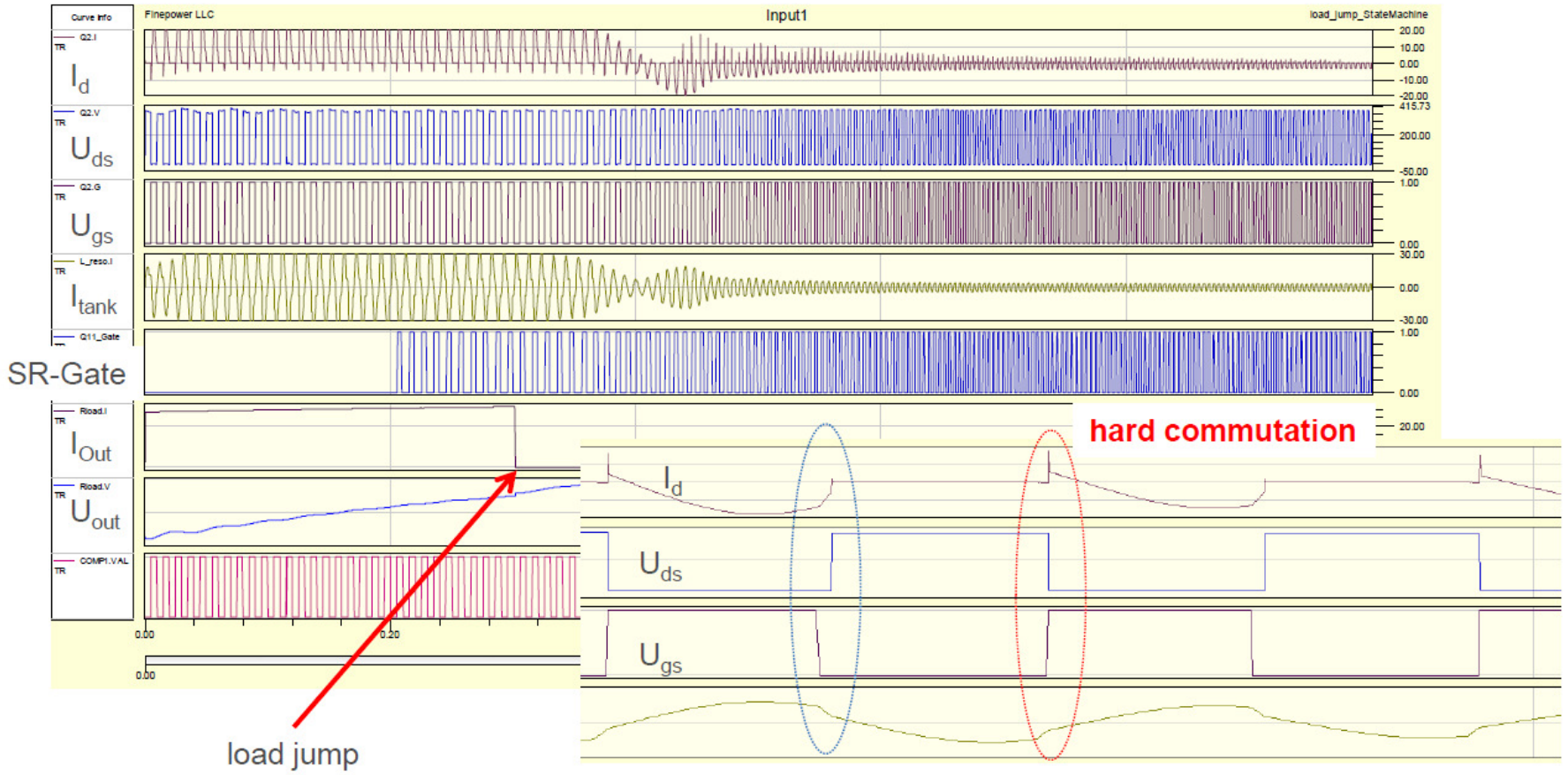
Load jump 100% to 0: SR activated



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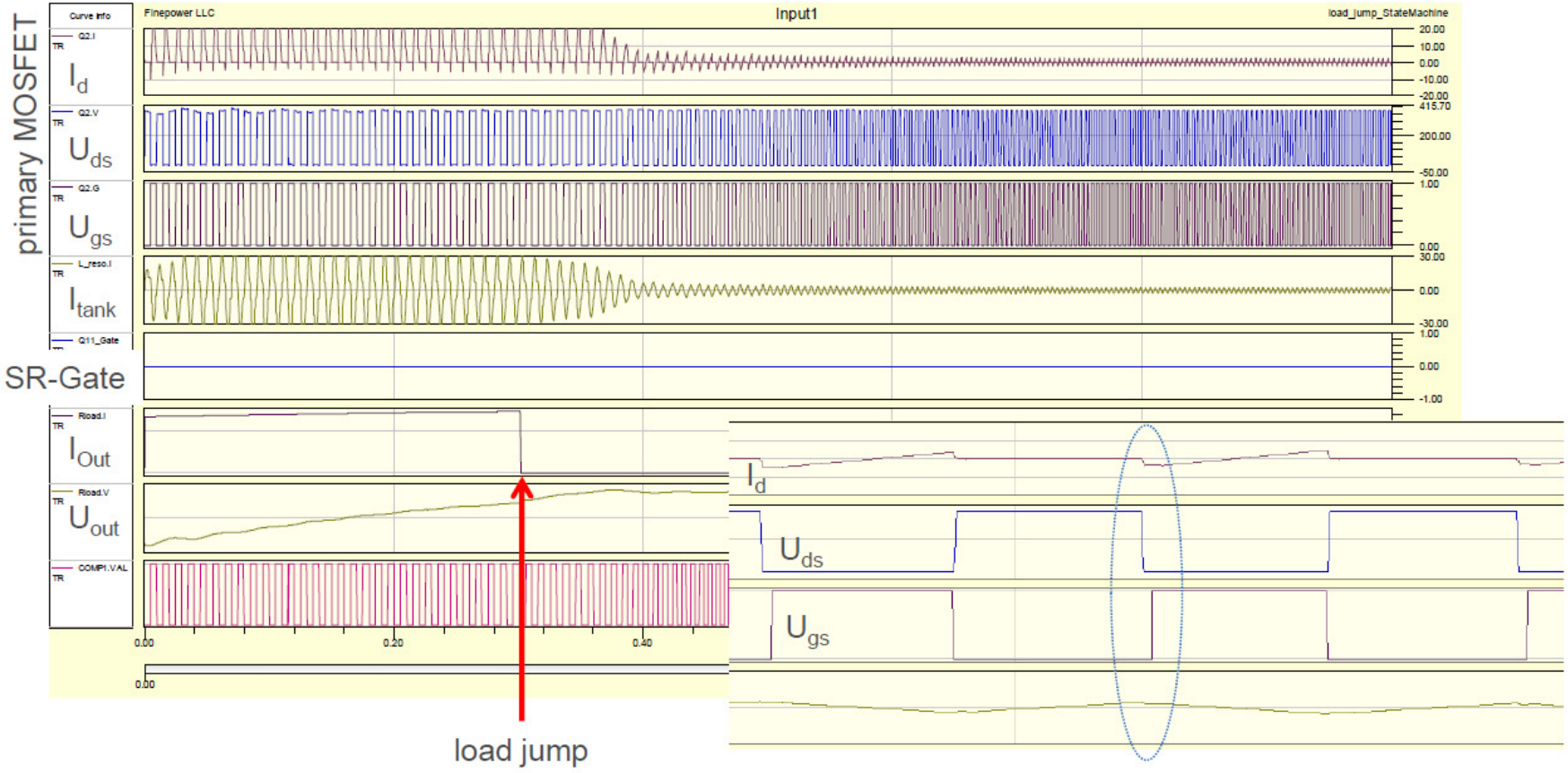
Load jump 100% to 0: SR de-activated



› If the current gradient between i[n-1] and i[n] is higher than a defined value this is a clear sign for load jump and the SR is deactivated

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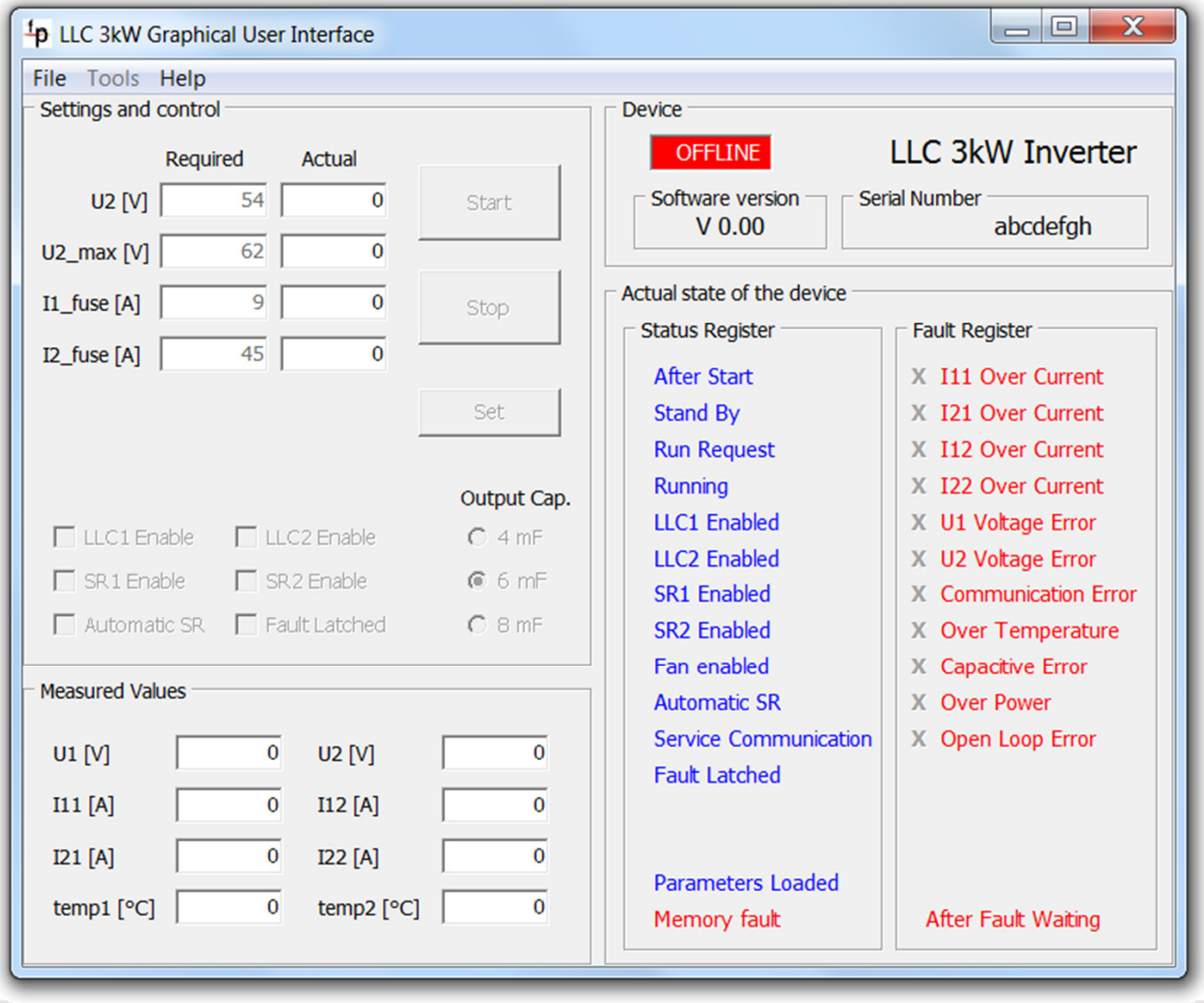
Graphical User Interface (GUI)

- GUI software controls the MCU by serial bus (UART) with TTL logic (3.3V).



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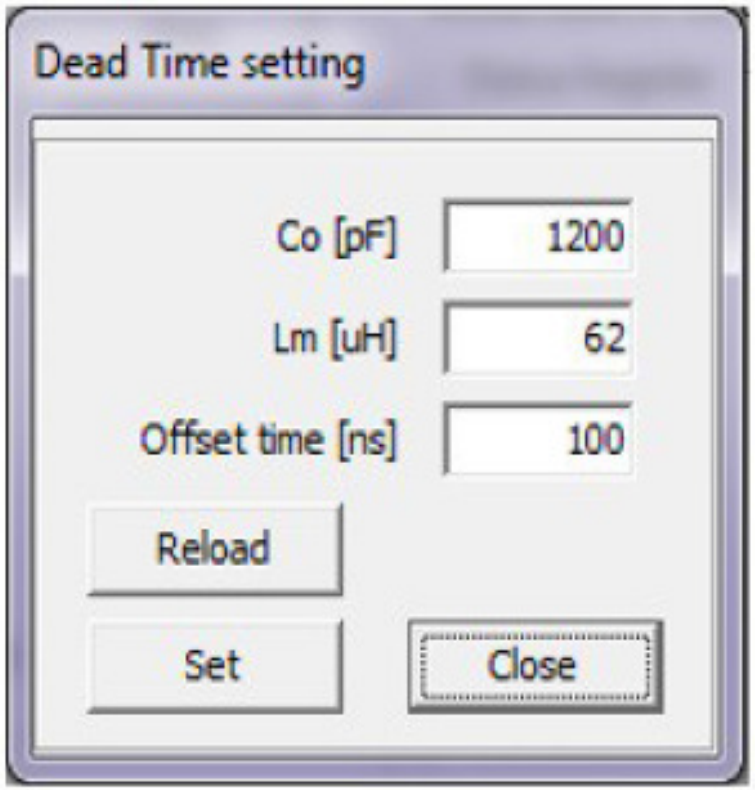
GUI: dead time setting



- Longer dead time is needed at light load/high line condition
- The amount of dead time depends on the FET Coss(tr) and the tank design. Although the resonant tank must be designed to assure enough energy for ZVS at all conditions, ZVS can be lost if the dead time is short.
- Given the designed tank and selected FETs, an equation is generated to relate dead time as function of switching frequency.

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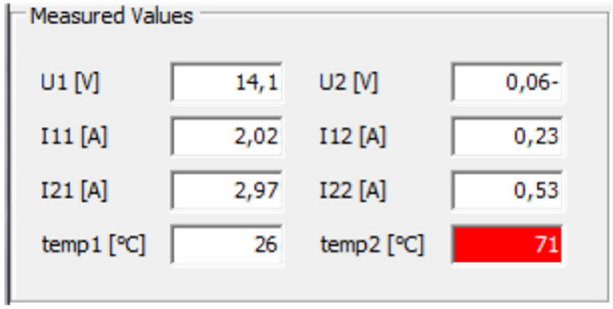
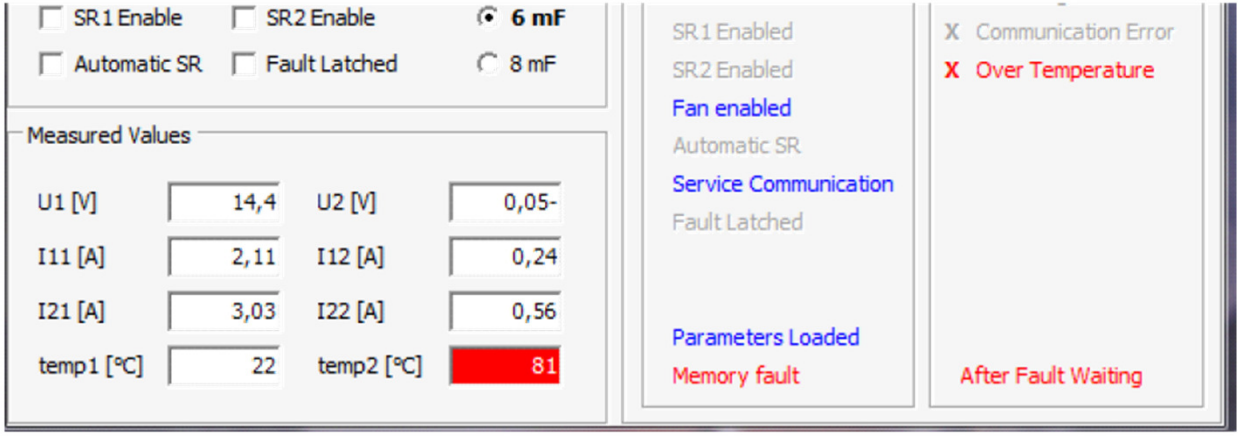
Temperature measurements and OT protection

GUI displays measured temperatures with white background when corresponding temperature is below 70°C or red when it exceeds 70°C. This temperature alarm doesn't effect LLC converter operation.



In case of system over-temperature (exceeding 80°C) MCU stops all power conversion and turns to fault state. This protection function is independent to GUI.



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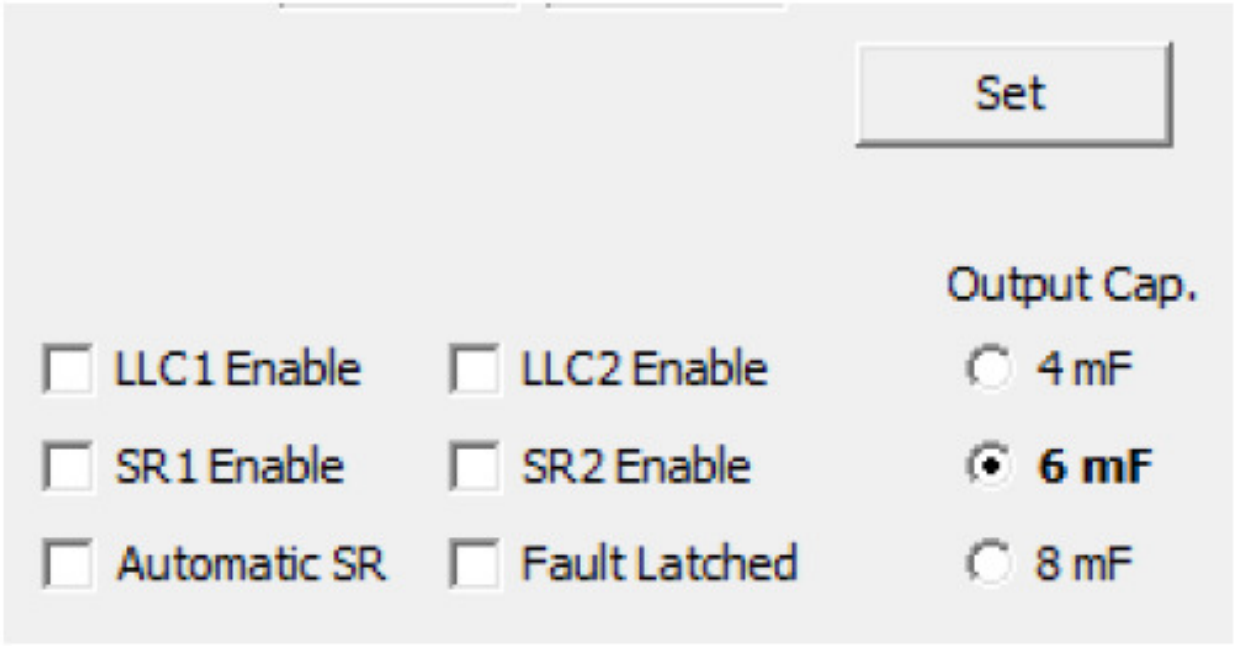
Automatic Loop Compensation



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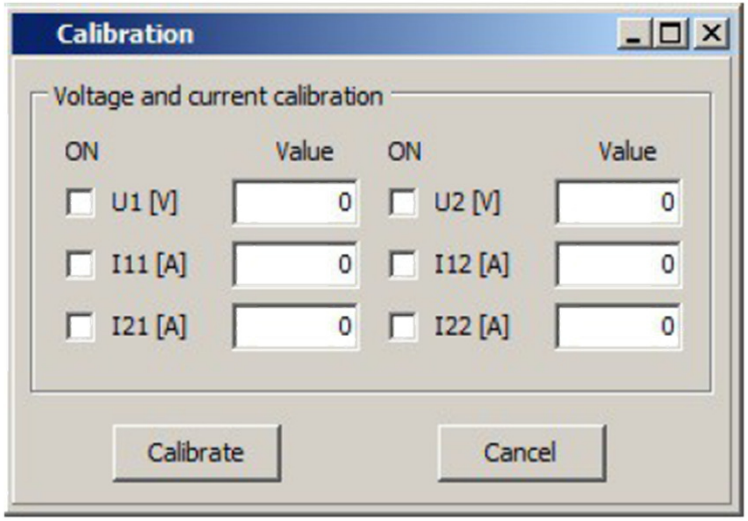
Calibration

- Tools → Calibration
- software provides offset calibration for currents and voltages
- operator only writes the actual correct value into the box, checks corresponding check-box and press "Calibrate" button



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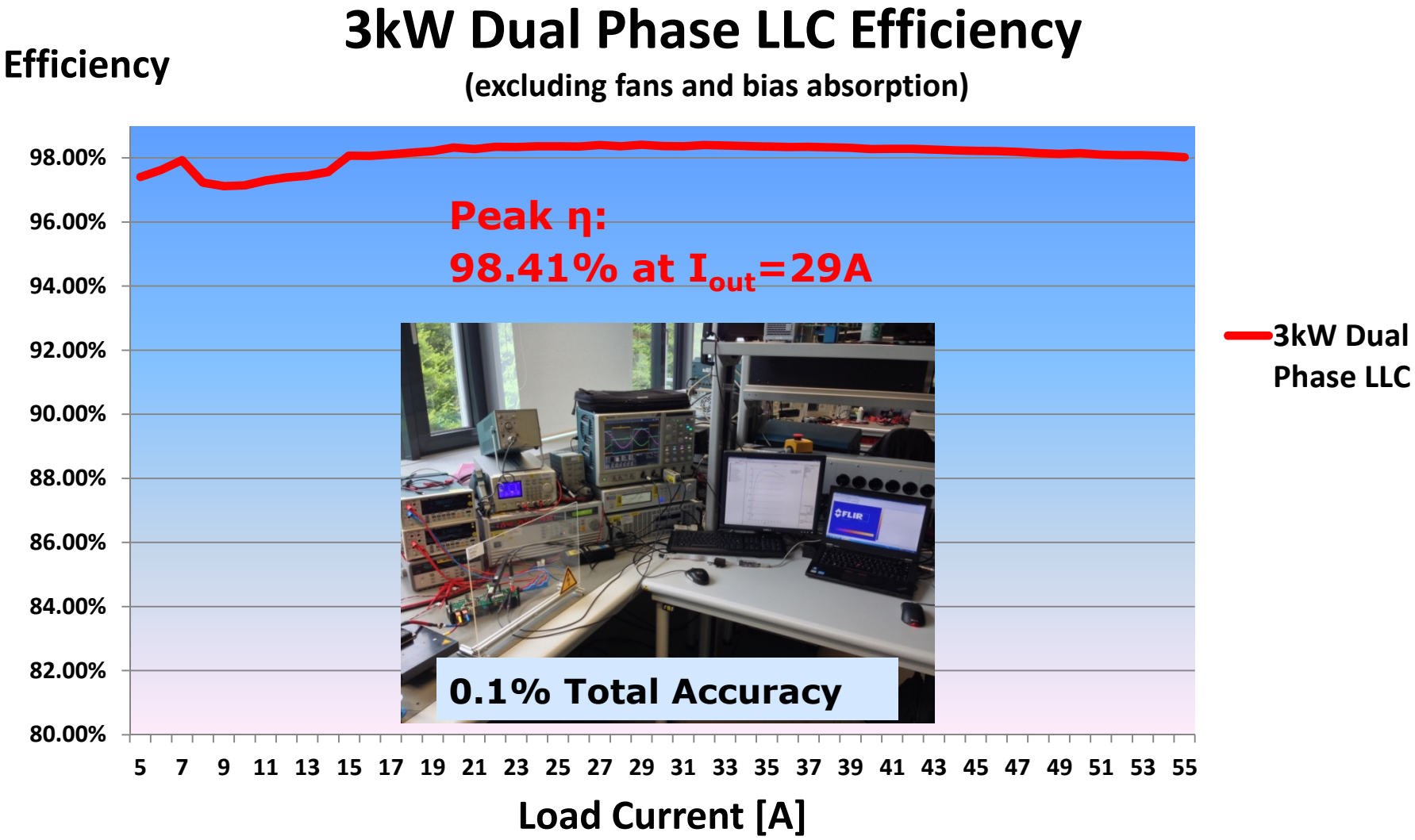
Efficiency Plot measured with IPW60R041P6 at Vin_nom=380VDC and Vout_nom=54.3VDC



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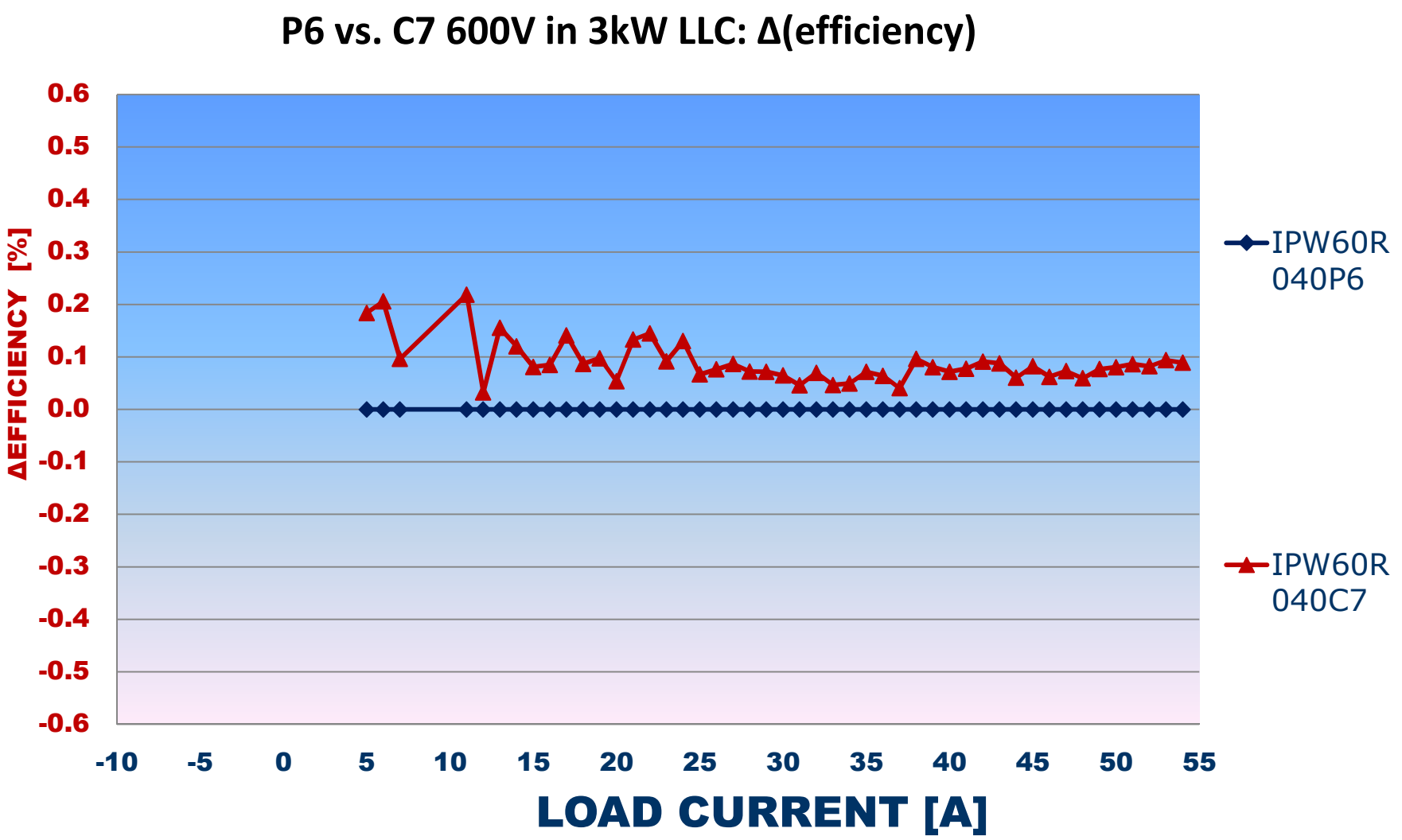
Δ(Eff) IPW60R041P6 vs. IPW60R040C7 at Vin_nom=380VDC and Vout_nom=54.3VDC



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